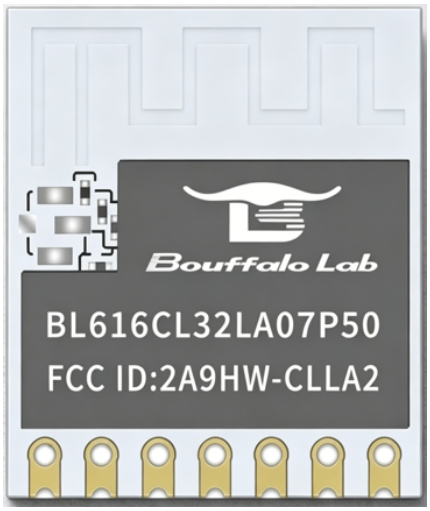
BL616CL32LA07P50

Module Specification



Module dimensions: 15.0 mm × 17.3 mm. The module integrates the BL616CL3250 chip, 2.4 GHz Wi-Fi (b/g/n/ax, 20 MHz bandwidth), Bluetooth Low Energy (BLE) 5.3, a CPU clock up to 320 MHz, 412 KB SRAM, and embedded 4 MB Flash. It supports 5 GPIOs, 5 PWM channels, two I2C interfaces, and two UART interfaces. An onboard PCB antenna is included.

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1 Module Overview

1.1 Overview

BL616CL is a highly integrated Wi-Fi 6 + Bluetooth 5.3 dual-mode low-power combo chip. It mainly consists of wireless and microcontroller subsystems. The wireless subsystem integrates 2.4 GHz RF, Wi-Fi 802.11b/g/n/ax, and BLE baseband/MAC. The microcontroller subsystem includes a low-power 32-bit RISC-V CPU with floating-point and DSP units, cache, and memory. The chip integrates a power management unit and supports multiple low-power modes and rich security features. Peripheral interfaces include SDIO, SPI, UART, I2C, USB2.0, PWM, ADC, DAC, and general-purpose GPIO.

The BL616CL system function block diagram is shown below:

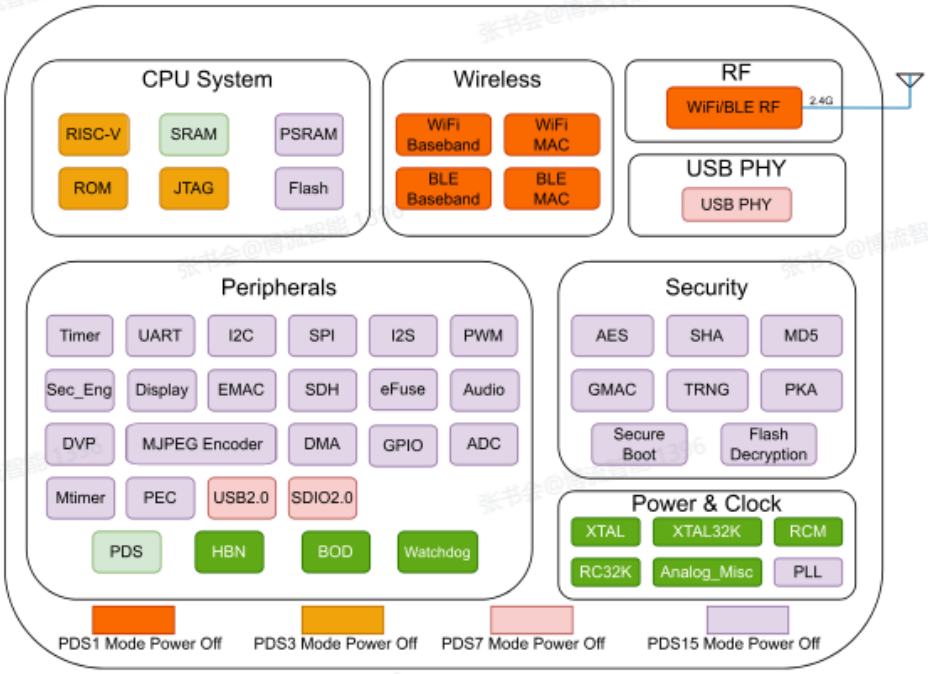

Figure 1: System Function Block Diagram

1.2 Key Features

- IEEE 802.11 b/g/n/ax (2.4 GHz, 1T1R), Bluetooth 5.3 (BLE)
- Wi-Fi 20 MHz bandwidth, 1T1R
- Wi-Fi security: WPS/WEP/WPA/WPA2/WPA3
- Supports STA, SoftAP, STA+SoftAP, and sniffer modes
- Smart provisioning and multi-platform cloud connectivity
- Supports fast Wi-Fi connection through BLE
- Supports on-chip Wi-Fi and BLE coexistence with a shared antenna
- Supports LDPC, STBC, Beamformee, DL/UL OFDMA, MU-MIMO, TWT (Target Wake Time), SR (spatial reuse), DCM (dual-carrier modulation), and ER (extended range)

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- Supports aggregation (AMPDU, AMSDU), immediate block acknowledgement, fragmentation, and defragmentation
- 412 KB available SRAM and embedded 4 MB Flash
- 5 GPIOs, configurable as UART, I2C, PWM, and other functions

1.3 Applications

- Internet of Things (IoT)
- Smart home
- Smart appliances
- Industrial lighting
- Smart sockets
- Smart panels
- Smart agriculture

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2 Module Specification

2.1 Functional Block Diagram

This module includes an onboard PCB antenna, and the RF matching parameters have already been tuned. End users can directly surface-mount the module in their finished products. The module functional block diagram is shown below:

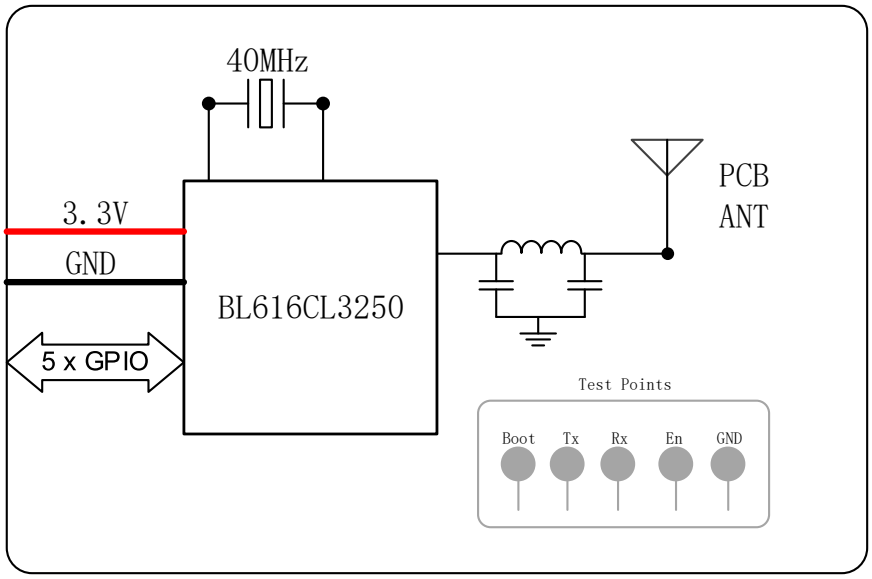

Figure 2: Module Functional Block Diagram

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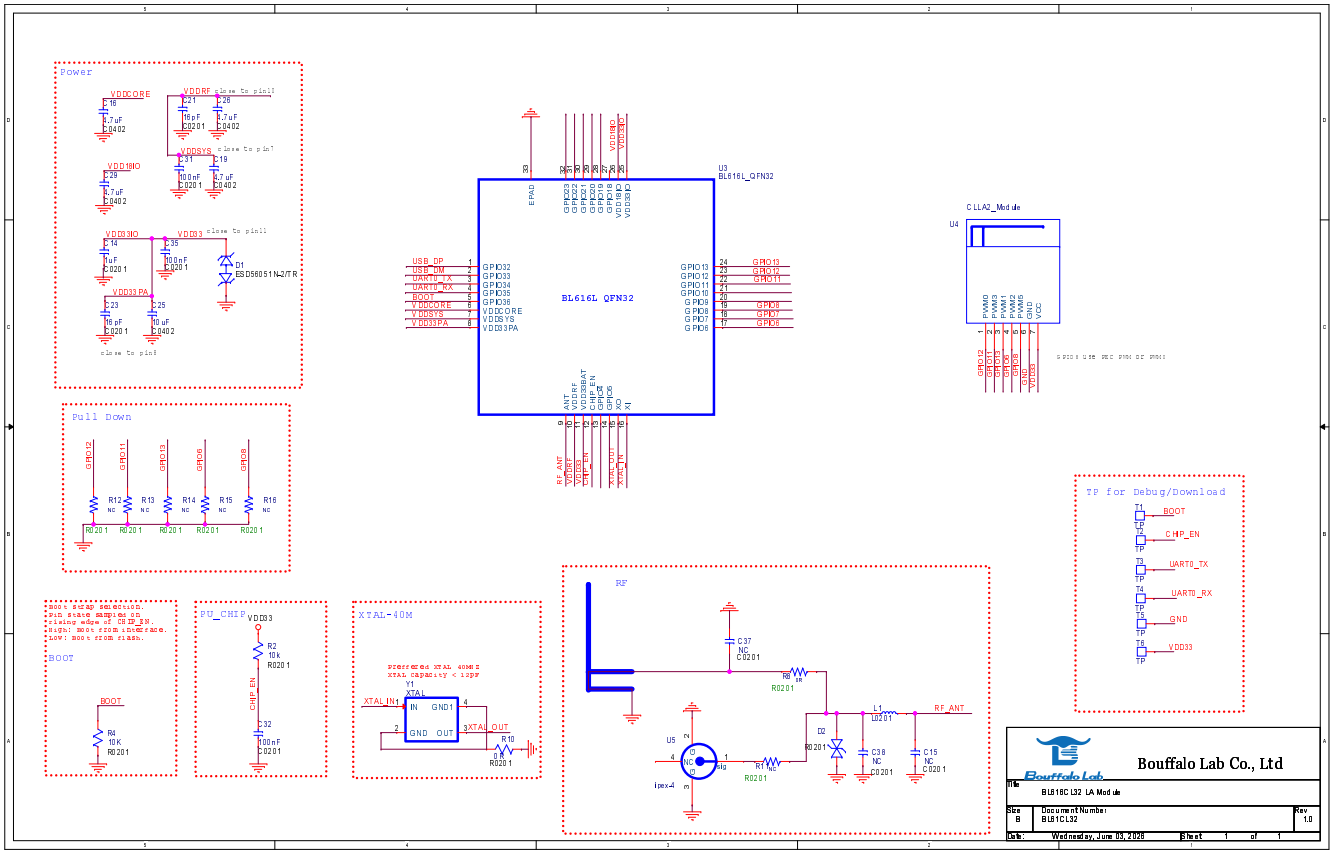
2.2 Schematic

The module schematic is shown below:



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BL616CL32LA07P50 Specification

2.3 Electrical Characteristics

2.3.1 Absolute Maximum Ratings

When using this module, users must ensure that the following conditions do not exceed the module's maximum ratings. Long-term operation beyond these ratings may cause reliability issues.

Table 1: Absolute Maximum Ratings

Parameter	Min	Max	Unit
Power supply voltage	-0.3	3.63	V
Operating temperature	-40	105	°C
Storage temperature	-45	135	°C
ESD protection (HBM)	2000	–	V

2.3.2 Recommended Operating Electrical Parameters

Table 2: Electrical Parameters (3.3 V, 25 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Power supply	VDD	2.9	3.3	3.6	V
I/O input low level	VIL	–	–	0.3*VDDIO	V
I/O input high level	VIH	0.7*VDDIO	–	–	V
I/O output low level	VOL	–	0.1*VDDIO	–	V
I/O output high level	VOH	–	0.9*VDDIO	–	V
I/O maximum source current	IMAX	–	25	–	mA
I/O maximum sink current	IMAX	–	23	–	mA
I/O internal pull-up/pull-down resistance	IMAX	–	35	–	kΩ

2.4 Wi-Fi RF Performance

Table 3: Wi-Fi RF Parameters

Parameter	Value
Frequency range	2400 - 2483.5 MHz

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Table 4: Wi-Fi Transmit Power (3.3 V, 25 °C)

Mode	Rate	Min	Typ	Max	Unit
11ax	mcs9	–	17	–	dBm
11ax	mcs0	–	20	–	dBm
11n	mcs7	–	18	–	dBm
11n	mcs0	–	21	–	dBm
11g	54m	–	19	–	dBm
11g	6m	–	21	–	dBm
11b	11m	–	23	–	dBm
11b	1m	–	23	–	dBm

Note: The typical transmit power values above are conducted measurement results obtained while meeting IEEE spectral mask and EVM requirements.

Table 5: Wi-Fi Receive Sensitivity (3.3 V, 25 °C)

Mode and Rate	Min	Typ	Max	Unit	Remarks
11b 1 Mbps	–	-100	–	dBm	–
11b 11 Mbps	–	-90	–	dBm	–
11g 6 Mbps	–	-93.5	–	dBm	–
11g 54 Mbps	–	-78	–	dBm	–
11n HT20 MCS0	–	-93	–	dBm	LDPC_OFF,LONG-GI
11n HT20 MCS7	–	-76	–	dBm	LDPC_OFF,LONG-GI
11ax HE20 MCS0	–	-93	–	dBm	LDPC_OFF,GI08
11ax HE20 MCS9	–	-67	–	dBm	LDPC_OFF,GI08

Note: The receive sensitivity test results above were measured by conducted testing using waveform files generated according to IEEE requirements.

2.5 BLE RF Performance

Table 6: BLE Transmit Power (3.3 V, 25 °C)

Rate Mode	Min	Typ	Max	Unit
1 Mbps	0	10	20	dBm
2 Mbps	0	10	20	dBm
S2 500 kbps	0	10	20	dBm
S8 125 kbps	0	10	15	dBm

Table 7: BLE Receive Sensitivity (3.3 V, 25 °C)

Rate Mode	Min	Typ	Max	Unit
1 Mbps	–	-99	–	dBm
2 Mbps	–	-96	–	dBm
S2	–	-101	–	dBm
S8	–	-104	–	dBm

2.6 Pin Definition

The module appearance is shown below. The left image is the module top side, and the right image is the module bottom side:

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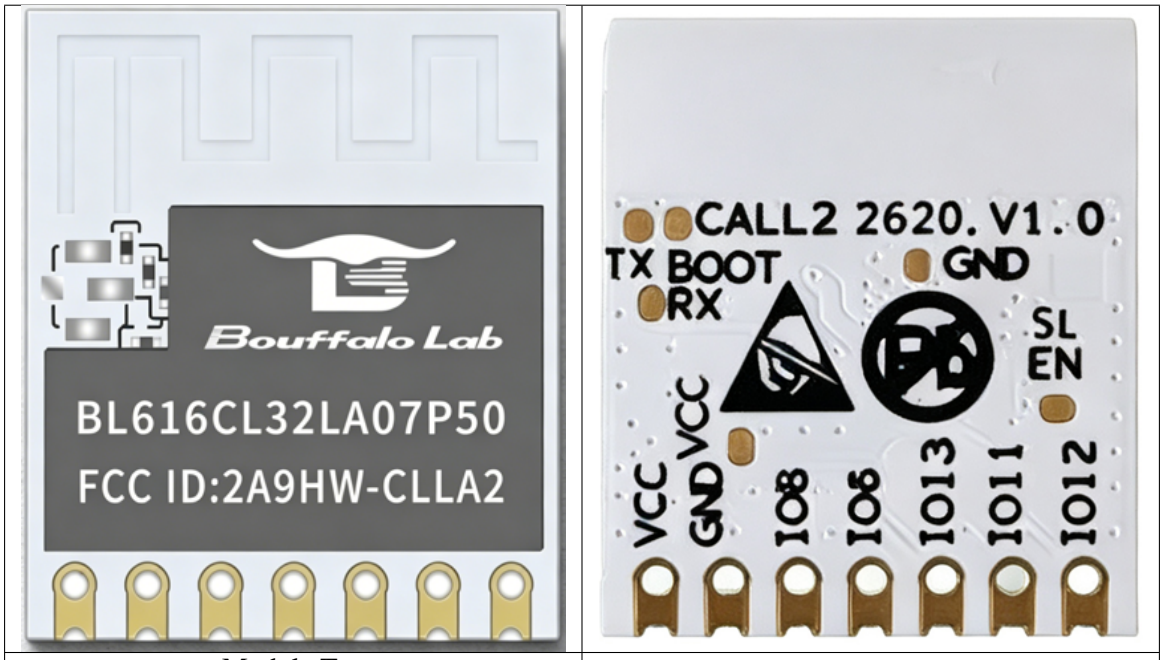

Module Top | Module Bottom

Figure 3: Module Appearance (Left: Top; Right: Bottom)

This module is highly integrated and provides 5 GPIOs for end users, as shown in the following table. The table also lists common I/O multiplexing functions.

Table 8: Pin Function Definition

No.	Name	Type	Description
1	GPIO12	I/O	GPIO12 / PWM0 / I2C_SCL
2	GPIO11	I/O	GPIO11 / PWM3 / I2C_SDA
3	GPIO13	I/O	GPIO13 / PWM1 / ADC_CH9
4	GPIO14	I/O	GPIO14 / PWM2 / UART_Tx
5	GPIO15	I/O	GPIO15 / PWM4 / UART_Rx
6	GND	Power	Ground
7	VCC	Power	Power supply 3.3 V

Note: In the module top view, the castellated pad at the lower-right corner is VCC (power input pin), and I/O indicates input/output pins. For other I/O multiplexing functions, refer to the chip manual.

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3 Application Notes

3.1 Schematic

- **Power supply**: It is recommended to connect a 10 μF capacitor and a 100 nF capacitor in parallel from the module 3.3 V power pin to GND. The 3.3 V power supply for the module should provide more than 500 mA current capability.
- **Enable/reset circuit**:
  - The reset enable circuit inside the module already includes a 10 kΩ resistor and a 100 nF capacitor. The default delay is 1 ms, and the module starts automatically after normal power-on.
  - If the end user needs to control module startup, the EN (CHIP_EN) test point on the back of the module can be routed out. It is recommended to reserve an additional pull-up resistor R and a parallel capacitor C.
- **Sleep wake-up**: Each reserved I/O on this module can be used as a sleep wake-up pin.
- **Input/output pins**:
  - Each reserved I/O on this module can be used as a general-purpose GPIO and can also be multiplexed as UART (not the download/debug interface), I2C, ADC, and other functions.
  - If the connected peripheral trace is long, a small resistor can be connected in series on the I/O signal line to prevent I/O voltage overshoot.
- **Download/debug interface**:
  - The module download/debug UART is available at the test points (Tx, Rx, Boot) on the back of the module and may be routed out as needed. To download firmware, connect Tx and Rx, pull the Boot pin high, and power on the module. For normal startup, leave the Boot test point floating (it is pulled down internally) and power on normally.
  - The module can be pre-programmed with the end customer's application firmware before shipment, so the user does not need to program firmware on their own production line.

3.2 PCB

- To ensure PCB onboard antenna performance, the module carrier board should include a large reference GND layer. A single-sided PCB is not recommended.
- The module power supply trace width should be greater than 30 mil, and the module should be well grounded. Avoid using 0 Ω resistors to bridge the ground connection. The capacitors connected in parallel to the power pin should be placed close to the module.
- The module includes its own PCB onboard antenna. Sufficient keep-out clearance must be reserved around the antenna. In addition, to expose the download/debug TP points on the back of the module, keep a 9.5 mm distance between the top end of the module and the carrier board, as shown below:

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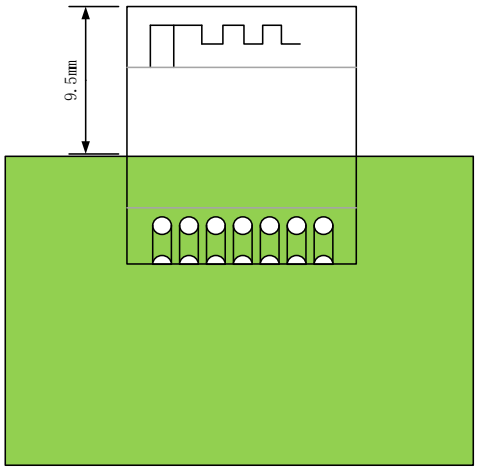

Figure 4: Recommended Layout 1

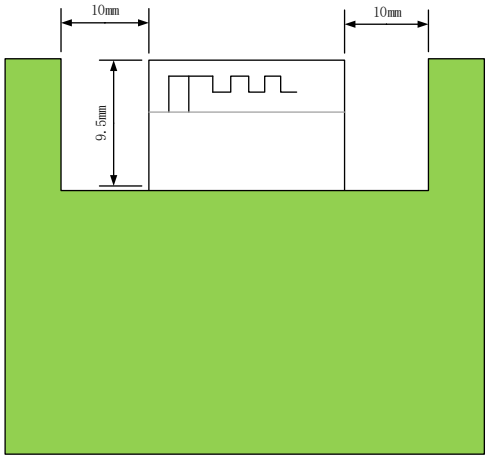

Figure 5: Recommended Layout 2

- Note that the TP points on the module bottom layer are exposed copper pads, so the corresponding carrier board area must not contain exposed copper to avoid short circuits.

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4 Dimensions and Footprint

Typical module dimensions (W × L × H):

15.0 mm × 17.3 mm × 2.8 mm, tolerance ± 0.1 mm

The detailed module dimensions are shown below:

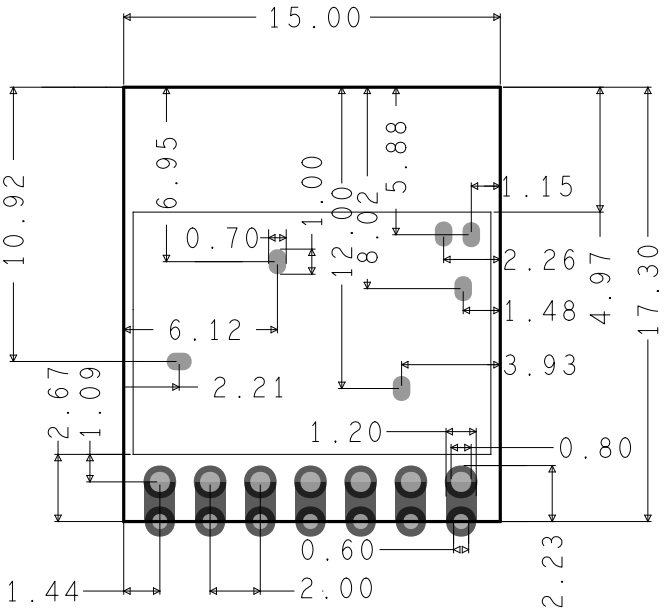

Figure 6: Detailed Module Dimensions

The recommended PCB footprint dimensions are shown below:

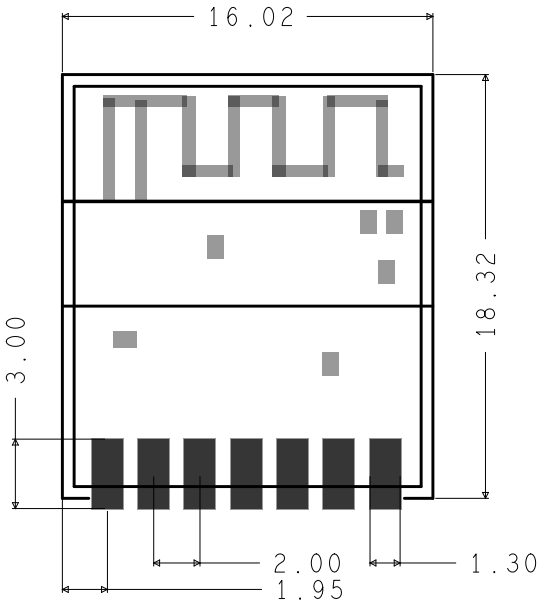

Figure 7: Module PCB Footprint Dimensions

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Note: Position the module so that its top edge is 9.5 mm from the edge of the carrier board, leaving the download/debug TP pads on the underside of the module exposed.

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5 Storage Conditions

- Sealed storage in a moisture-proof bag: temperature < 40 °C, humidity < 90 %RH
- Moisture sensitivity level: MSL3
- After opening: use within 168 hours under 25 ± 5 °C / 60%RH conditions; otherwise, rebaking is required

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6 Recommended Reflow Profile

- Peak temperature: < 250 °C
- Soldering cycles: ≤ 2 times
- Ramp-up slope: maximum 1~2 °C/s
- Preheat: 150~200 °C, 60~120 s
- Cooling rate: maximum 2.5 °C/s above 217 °C

The recommended reflow temperature profile is shown below:

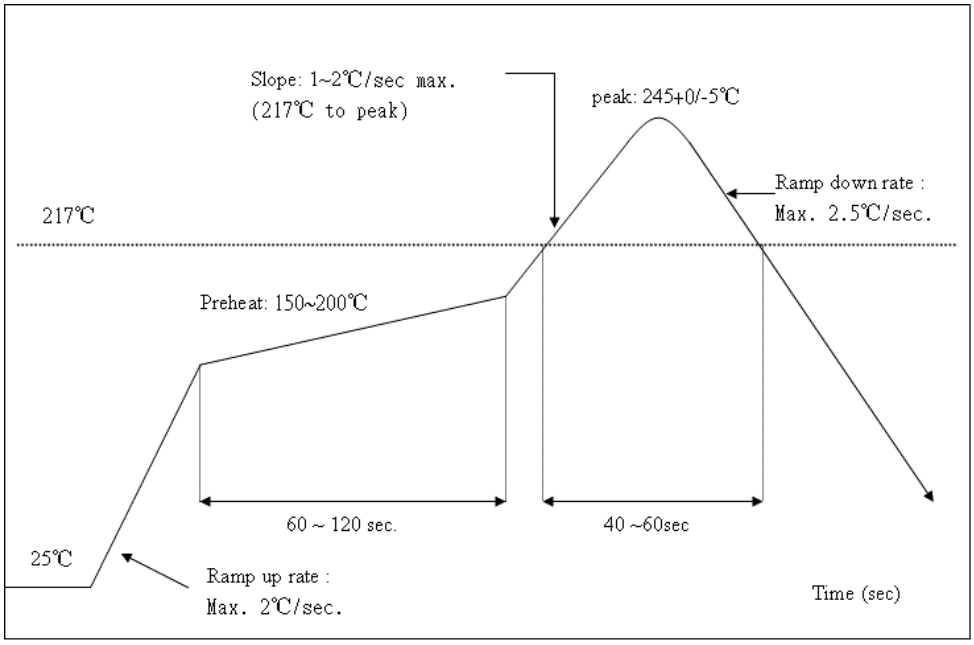

Figure 8: Reflow Temperature Profile

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7 Contact Information

- Website: `https://www.bouffalolab.com`
- Forum: `https://bbs.bouffalolab.com`
- Open-source community: `https://github.com/bouffalolab`
- Business: info@bouffalolab.com
- Technical support: support@bouffalolab.com

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9 Revision History

Version	Date	Author	Changes
V1.0	2026-04-01	Bouffalo Lab	Initial version
V1.1	2024-05-15	Bouffalo Lab	Updated RF parameters
V1.2	2024-06-20	Bouffalo Lab	Updated pin definitions
V1.3	2024-07-01	Bouffalo Lab	Updated electrical characteristics

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