Data Sheet



BL618DG DataSheet

Apr. 2026

Features

- Wi-Fi
  - 2.4/5GHz Dual-Band 1x1 射频收发器
  - Wi-Fi 6 (IEEE 802.11 b/g/n/ac/ax)
  - 支持 1024-QAM Modulation (MCS11)
  - 支持 20/40MHz 带宽, 1T1R
  - 支持 WPS/WEP/WPA/WPA2/WPA3
  - 支持 LDPC, STBC, Beamforming, DL/UL OFDMA, MU-MIMO, TWT (Target Wake Time), SR (Spatial Reuse), ER (Extended Range)
  - 支持 Aggregation (AMPDU, AMSDU), Immediate Block Ack, Fragmentation, Defragmentation
  - 支持 Support IEEE 802.11e QoS WMM (Wi-Fi Multi-Media), IEEE 802.11w PMF (Protected Management Frames), IEEE 802.11z TDLS, IEEE 802.11h DFS TPC, IEEE 802.11r
  - 支持 STA, Soft-AP, STA + Soft-AP 和 sniffer 模式
  - 集成 RF balun, PA/LNA
- BLUETOOTH 5.3 和 IEEE 802.15.4
  - 蓝牙 ® 5.3 双模 (BT+BLE)
  - 支持 IEEE 802.15.4(Matter/Zigbee/Thread)
  - 支持 Wi-Fi, BT/BLE and Zigbee 共存
- 微控制器子系统
  - HP RISC-V processor AP & NP
    - 时钟频率: AP 640MHz, NP 480MHz
    - 支持 FPU
    - 9 级流水线
    - 支持 RISC-V RV32IMAFC 指令集
    - 32KB I-Cache, 两路组相连结构
    - 32KB D-Cache, 两路组相连结构
    - 支持 RISC-V Debug 协议标准
  - 支持 NOR FLASH XIP
- 音频编码译码器
  - Audio ADC*1 (MIC, SNR>TBD dB)
  - Audio DAC*1 (Speaker, SNR>TBD dB)
  - 时钟来自 WiFi PLL 和 CPU PLL
- Memory
  - 总计 852K SRAM
    - 320K OCRAM
    - 320K WRAM
    - 128K MRAM
    - 16K XRAM
    - 64K BT/BLE RAM
    - 4K HBN RAM
  - 支持内置/外置 Nor FLASH
  - 支持内封 PSRAM
- Video/Image/Display
  - Camera Sensor DVP 接口

  - LCD 显示接口 (DBI-C, DBI-B, RGB 和 MIPI DSI)
  - OSD（On-Screen Display）
  - MJPEG encoder
  - MJPEG decoder
- 安全
  - 安全启动 (支持固件加密 & 签名)
  - 安全调试
  - 支持 Anti-Rollback
  - XIP On-The-Fly AES 解密 (OTFAD)
  - 支持 TrustZone
  - AES-ECB/CBC/CTR/XTS 模式
  - SHA-1/224/256/384/512
  - TRNG（真随机数生成器）
  - 用于 RSA/ECC 的 PKA（公钥加速器）
  - 总计 4096 bits eFuse
- 外设
  - 2 路 EMAC, 支持 1588 协议
  - 1 路 USB 2.0 HS，支持主机/设备模式
  - SDIO3.0 主机
  - SDIO3.0 从机
  - 3 路 DMA，共 20 通道（8+8+4）
  - 4 路 UART（支持 5V IO）
  - 3 路 I2C，支持主机模式
  - 4 路 SPI，支持主/从模式
  - 2 路 IPC
  - 2 路 GPTimer
  - 2 路 GPADC（每路支持 12 个外部 channel）
  - 1 路 I2S，支持主/从模式
  - 2 路 PWM, 每路包含 4 个通道
  - 3 路 CAN FD
  - 1 路 KeyScan
  - 1 路 IR(TX & RX)
  - 1 路 TOUCH，可在自扫描模式对最高 8 路通道扫描
  - 1 路 PEC(Peripherals Expander Controller)
- 时钟
  - 支持 XTAL 40/52MHz
  - 支持 XTAL 32.768KHz
  - 内部 RC 32KHz /32MHz 振荡器
  - 两路 PLL, WiFi PLL & CPU PLL
- 封装类型
  - QFN56
  - QFN68

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1 概述

BL618DG SoC 集成了 2.4G 和 5G 双频 WiFi6，同时支持 BT/BLE 以及 IEEE802.15.4，具有丰富的外设，可以满足 AIoT，新能源等多种应用领域的要求。

BL618DG 支持 IEEE 802.11a/b/g/n/ax，2.4G 频段支持 20/40 MHz 带宽以及 1024 QAM 调制，5G 频段支持 20/40MHz 带宽以及 1024 QAM 调制。*BL618DG* 同时集成了 2.4G 频段的 BT/ BLE 以及 IEEE802.15.4。WiFi 与 BT/ BLE/ IEEE802.15.4 使用独立天线的设计满足了共存需求。

在电源管理上，*BL618DG* 内部集成了一路 DCDC 以及 2 路 LDO，外部只需单路 3.3V 供电，简化外围电源设计。

BL618DG 集成了 2 个高性能 RISCV CPU，拥有丰富外设，包括: Timer /UART /I2C /SPI /PWM /IPC /Sec_Eng /EMAC /KeyScan /IR / Audio/ I2S/ TOUCH /CAM /MJPEG_Encoder /MJPEG_Decoder /OSD /Display /ADC /SDIO3.0 (Host&Device) /USB2.0 /DMA 等。

BL618DG 支持安全启动，支持镜像加密和签名，支持固件反回滚 (anti-rollback)，满足智能家电，物联网，新能源等领域的各种安全应用需求。

芯片的功能框图如下图所示。

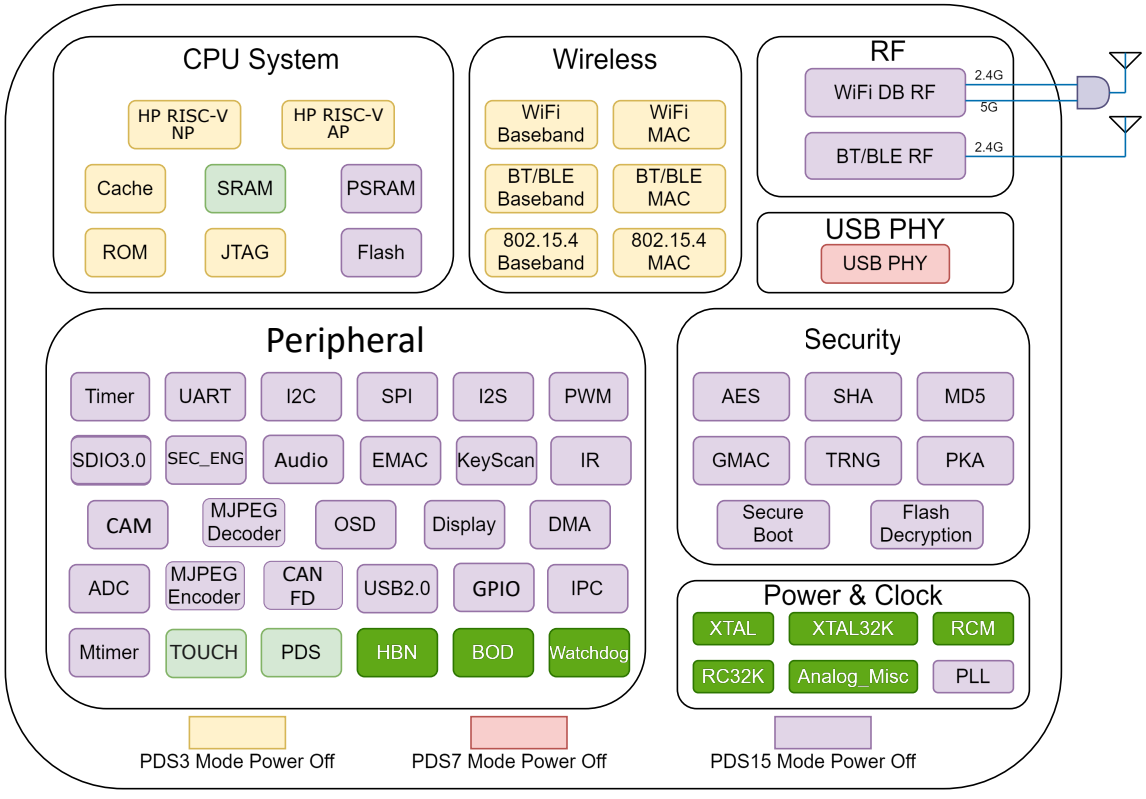

图 1.1: 功能框图

2 功能描述

BL618DG 系统架构如下所示:

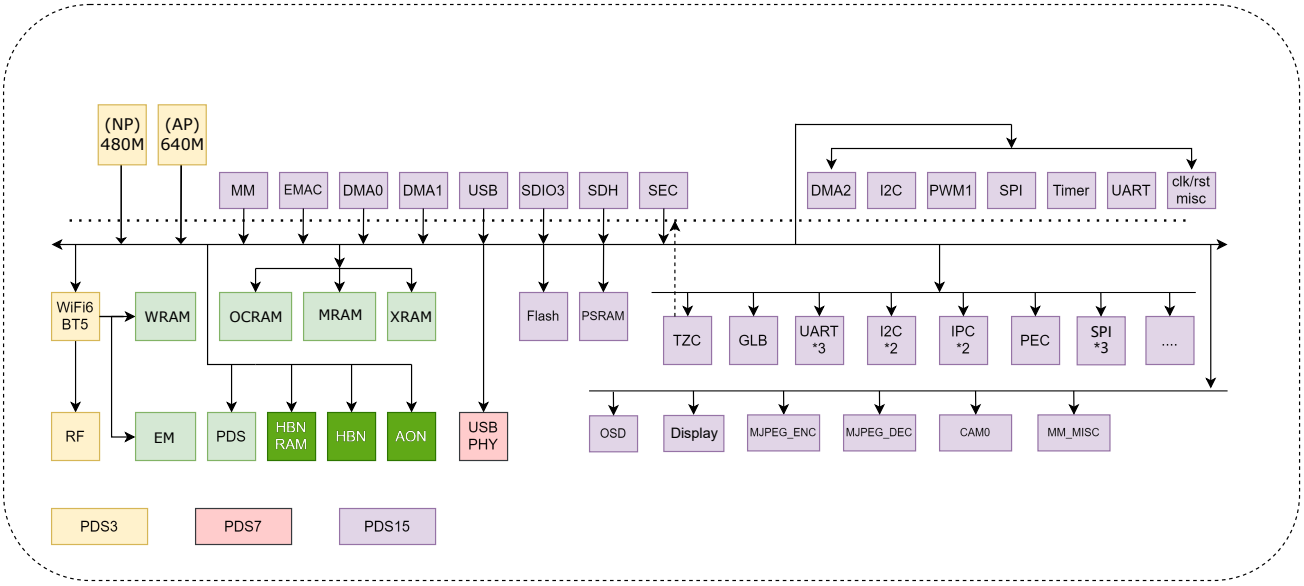

图 2.1: 系统架构图

CPU 带有 AXI 和 AHB 两条总线，ROM，Flash 和 PSRAM 挂在 AXI 总线上，以实现对这些存储单元的高速访问，各个外设通过 AHB 总线与 CPU 连接在一起。

2.1 CPU

BL618DG 集成了 2 个高性能 RISCV CPU(AP & NP)。

AP/NP 采用 9 级流水线结构：取指、译码、执行、访存、写回，其中取指和访存阶段都分别包含了 3 级流水线。支持 RISC-V 32/16 位混编指令集，包含外部中断源，有 3 个 bits 可以用于配置中断优先级。

2.2 缓存

BL618DG 的高性能处理器 NP 和 AP 均拥有一个一级缓存（L1 Cache），包含 32K 指令 cache 和 32K 数据 cache。

2.3 内存

BL618DG 的内存包括：320K OCRAM，用于 NP 的应用程序;320K WRAM，用于 WiFi 无线数据的收发；128K MRAM，用于 AP 的应用程序；16K XRAM，用于两个 CPU 通信；64K ERAM，用于 BT/BLE 无线数据的收发；4K HBN RAM，用于 PDS/HBN 模式下保存低功耗数据。上述各个 RAM 的访问不受 CPU 的限制，即每个 CPU 都可以对上述 RAM 发起读写访问。此外，*BL618DG* 还支持内封 PSRAM。

2.4 DMA 控制器

BL618DG 有 3 路 DMA（直接存储器访问），总计 20 个通道，用于管理外设和存储器之间的数据传输，以提高 CPU /BUS 效率。DMA 有四种传输类型，内存到内存，内存到外设、外设到内存以及外设到外设四种模式。DMA 还支持 LLI（链接列表项）功能，该链表由一系列链接列表预定义多个传输，然后硬件会根据每个 LLI 的大小和地址自动完成所有传输。DMA 支持的外设包括 UART、I2C、IR、SPI、Audio、I2S、GPIO、DBI、GPADC 等。

2.5 地址映射

表 2.1: 内存地址映射

模块	大小	开始地址	
		Cache	Non-cache
OCRAM	320KB	0xA1000000	0x21000000
WRAM	320KB	0xA1050000	0x21050000
MRAM	128KB	0xA10A0000	0x210A0000
XRAM	16KB	0xA10C8000	0x210C8000
HBN RAM	4KB	X	0x20090000

OCRAM/WRAM/MRAM/XRAM 既可以通过 AHB 总线访问，也可以通过 AXI 访问，当 CPU 使用 0xAXXXXXXX 地址访问时，会经过内部 Cache 并通过 AXI 转 AHB 实现对各个 RAM 的访问，当 CPU 使用 0x2XXXXXXX 地址访问时，不会经过内部 Cache，直接通过 AHB 总线访问。

表 2.2: 地址映射

模块	目标	开始地址	大小	描述
FLASH	Flash	0xA0000000		应用程序地址空间
PSRAM	pSRAM	0xA8000000		pSRAM 存储器地址空间 (可选项，依赖芯片具体型号)
	HBN	0x2008F000	4KB	深度睡眠控制（休眠）寄存器

表 2.2: 地址映射 (continued)

模块	目标	开始地址	大小	描述
	PDS	0x2008E000	4KB	睡眠控制（掉电睡眠）寄存器
	EMAC_1	0x2008C000	8KB	EMAC 控制寄存器
	EMAC_0	0x2008A000	8KB	EMAC 控制寄存器
	USB	0x20087000	4KB	USB High Speed OTG 控制寄存器
	SDU	0x20085000	4KB	SDIO Device 控制寄存器
	SDH	0x20084000	4KB	SDIO Host 控制寄存器
	SF_Ctrl	0x20082000	4KB	Serial Flash 控制寄存器
	DMA0	0x20081000	4KB	DMA0 控制寄存器
	SEC_ENG	0x20080000	4KB	安全引擎控制寄存器
	PEC	0x2001F000	4KB	外设扩展控制寄存器
	SPI2	0x20023000	4KB	I2S 控制寄存器
	AUDAC	0x20022000	4KB	AUDAC 控制寄存器
	DMA1	0x20021000	4KB	DMA1 控制寄存器
	I2S	0x2001E000	4KB	I2S 控制寄存器
	CKS	0x2001C000	4KB	CKS 控制寄存器
	DBI	0x2001D000	4KB	DBI 控制寄存器
	IRR	0x2001B000	4KB	IR Remote 控制寄存器
	TIMER0	0x2001A000	4KB	TIMER0 控制寄存器
	PWM0	0x20019000	4KB	PWM0 控制寄存器
	SPI1	0x20018000	4KB	SPI1 控制寄存器
	AUADC	0x20017C00	4KB	AUADC 控制寄存器
	IPC1	0x20016000	4KB	IPC1 控制寄存器
	I2C1	0x20015000	4KB	I2C1 控制寄存器
	I2C0	0x20014000	4KB	I2C0 控制寄存器
	IPC0	0x20013000	4KB	IPC0 控制寄存器
	UART2	0x20012000	4KB	UART2 控制寄存器
	UART1	0x20011000	4KB	UART1 控制寄存器
	UART0	0x20010000	4KB	UART0 控制寄存器
	KYS	0x2000F800	2KB	KeyScan 控制寄存器
	CAN2	0x2000F000	2KB	CAN2 控制寄存器
	CAN1	0x2000E800	2KB	CAN1 控制寄存器
	CAN0	0x2000E000	2KB	CAN0 控制寄存器
	PSRAM_Ctrl	0x2000D000	4KB	PSRAM 控制寄存器
	Efuse	0x2000C000	4KB	Efuse 存储控制寄存器

表 2.2: 地址映射 (continued)

模块	目标	开始地址	大小	描述
	SPI0	0x2000B000	4KB	SPI0 控制寄存器
	TZ	0x20006000	4KB	TrustZone 控制寄存器
	DMA2D	0x20005000	4KB	DMA2D 控制寄存器
	GPIP	0x20002000	4KB	通用 ADC 接口控制寄存器
	GLB	0x20000000	4KB	全局控制寄存器
	OSD	0x2004A000	4KB	OSD 控制寄存器
	DVP_RASTER	0x20046000	8KB	图像旋转与镜像控制寄存器
	DPI	0x20045000	4KB	DPI 控制寄存器
	MJDEC	0x20044000	4KB	MJPEG 图像解码控制寄存器
	MJPEG	0x20043000	4KB	MJPEG 图像编码控制寄存器
	CAM	0x20041000	8KB	CAM 摄像头接口控制寄存器
	DMA2	0x000C0000	4KB	DMA2 控制寄存器
	SPI3	0x00085000	4KB	SPI3 控制寄存器
	UART3	0x00084000	4KB	UART3 控制寄存器
	TIMER1	0x00083000	4KB	TIMER1 控制寄存器
	I2C2	0x00082000	4KB	I2C2 控制寄存器
	PWM1	0x00081000	4KB	PWM1 控制寄存器

2.6 中断

BL618DG NP/AP CPU 支持 UART/I2C/SPI/Timer/DMA/EMAC/WiFi/BLE 等可屏蔽中断触发源。

所有 I/O 引脚都可以配置为外部中断输入模式，外部中断支持同步高/低电平触发、同步上升沿/下降沿触发、异步高/低电平触发、异步上升沿/下降沿触发和同步双边沿触发共 9 种触发类型。

2.7 启动选项

BL618DG 支持多种启动选项，可选择从 Flash/UART/ USB/ SDIO 启动。

表 2.3: 启动模式

启动引脚	电平	描述
GPIO33	1	从 UART(GPIO11/12 或者 11/42)/USB(GPIO40/41)/SDIO 启动，该模式主要用于 Flash 烧写或者下载镜像到 RAM 执行 (无线透传场景)
	0	从 Flash 启动应用镜像

2.8 时钟架构

TBD

2.9 外设

2.9.1 GPIO

GPIO 口支持用作普通 GPIO 输入，输出，中断等功能外，可以复用为外设和模拟功能：

- 每个 GPIO 都可用作通用输入和输出功能，上拉/下拉/浮空可由软件配置
- 每个 GPIO 都支持中断功能，中断支持同步高/低电平触发、同步上升沿/下降沿触发、异步高/低电平触发、异步上升沿/下降沿触发和同步双边沿触发
- 每个 GPIO 均可设置为高阻态，用于低功耗模式
- 每个 GPIO 均可通过 Set/Clear 寄存器完成输出状态的控制
- 支持自定义的逻辑 0/1 波形输出
- 支持 DMA

2.9.2 EMAC

BL618DG 内置两路以太网 EMAC(Ethernet Media Access Controller)，兼容 IEEE 802.3 的 10/100Mbps，支持 IEEE 1588，MAC 与以太网 PHY 通过 RMII 接口进行通信，接口时钟需来自 PHY 的 50M 时钟输出。具有以下功能特性：

- 兼容 IEEE 802.3 定义的 MAC 层功能
- 支持 IEEE 802.3 定义的 RMII 接口的 PHY
- 通过 MDIO 接口与 PHY 交互
- 支持 10Mbps 与 100Mbps 以太网

- 内置 DMA 控制器实现根据收发描述符完成高速数据搬运
- 支持 IEEE 1588 协议
- 支持 VLAN
- 支持半双工与全双工工作模式
- 支持 CRC 的生成及校验
- 支持巨型帧
- 广播包过滤
- 发送/接收的各种事件标志
- 在事件发生时产生对应中断

2.9.3 USB

BL618DG 内置一路 USB2.0 高速控制器和 PHY，控制器和 PHY 之间通过 UTMI 接口通信，支持全速 (12 Mbit/s) 和高速 (480Mbit/s) 模式，兼容 USB2.0 协议，支持 suspend 和 resume 等特征。USB 主要功能特点如下：

- 支持 Host/Device 模式
- 内嵌 USB PHY
- 支持 8+1 个双向端点
- 支持 8 个 512 Bytes FIFO 与一个端点 0 专用的 64 Byte FIFO
- 支持 1 个端点绑定 1 个或者多个 FIFO
- 支持 USB 2.0 LPM (Link Power Management)
- 内部集成 USB VDMA

2.9.4 SDIO3.0 Host

SDH 是 SD 总线接口主机控制器，用于控制与管理 SD 存储卡、SDIO 卡等设备，提供数据存储和扩展功能。具有以下特点：

- 符合 SD Host Controller Standard Specification Version 3.0
- 符合 Compliant to SD 3.0 Physical Layer Specification Version 3.01
- 符合 Compliant to SDIO Specification Version 3.0

- 支持 DS/HS 速率与 UHS-I 标准的 SDR12/SDR25/SDR50/SDR104 速率
- 支持 Clock Tuning 功能，支持 ADMA2

2.9.5 SDIO3.0 Device

BL618DG 集成了一路 SD 设备接口，兼容 SDIO3.0 标准，支持 SDIO 主机通过 SDIO 总线接口和协议访问访问芯片内部的 SDIO 部分寄存器和 RAM。SDIO 内部集成 ADMA。具有以下特点：

- 支持 SPI/1-bit/4-bit 传输模式
- 最大时钟频率支持 208MHz
- 支持基于内嵌 DMA 的数据收发
- 支持命令/传输状态等多种中断
- 支持高速通信时序 tuning

2.9.6 CAM

CAM 用于图像传感器与 ‘BL618DG‘ 之间传输图像数据，具有以下特性：

- 8-bit 并行数据位宽
- 支持 YUV444/RGB888(24-bit)、YUV422/RGB565(16-bit)、YUV400(8-bit) 等数据格式输入并按原格式输出
- 支持将 RGB888 输入格式转为 RGB565/RGBA8888 格式输出
- 支持将 YUV422 输入格式转为 YUV420/400 格式输出
- 可配置的行帧同步信号选择和极性选择
- 支持图像矩形裁剪
- 以 1~32 为周期的帧取舍功能
- 支持行帧同步信号的完整性检测
- 支持完成中断

2.9.7 MJPEG Encoder

MJPEG 编码器用于对未压缩的图像数据流进行编码，支持以下特性：

- 输入数据流支持直接从 RAM 中读取或与 DVP 进行同步，可以直接对 DVP 采集到的 YUV 数据进行压缩
- 输入图像支持 YUV420SP、YUV400、YUV422SP、YUV422I 图像色彩空间
- 支持使能/禁止的 JPEG 文件头自动复制功能
- 两个可编程量化表
- 输出数据流支持双缓冲
- 仅支持标准 huffman 编码表
- 支持的中断包括：一帧压缩完成、双缓冲模式的缓冲区满

2.9.8 MJPEG Decoder

MJPEG 解码器用于对压缩的图像数据流进行解码，支持以下特性：

- 输出图像支持 YUV420SP、YUV400、YUV422SP 图像色彩空间
- 支持使能/禁止自动跳过 JPEG 文件头的功能
- 两个可编程量化表
- 支持自定义 huffman 编码表
- 支持解码完成后产生中断

2.9.9 DBI

DBI(Display Bus Interface) 模块拥有 8 位并行数据线，用于驱动带有显存的屏幕显示，具有以下特性：

- 支持 Type-B (8-bit)、Type-C Option 1 (3-wire) 以及 Type-C Option 3 (4-wire) 模式
- 支持 RGB565/666/888 输出格式
- 支持 QSPI 模式，QSPI 的 CMD/ADDR/DATA 可任意选择 1-/4-wire 模式
- 支持 RGB565/RGB888/RGBA8888/YUV444 输入格式
- 支持 DMA 功能

2.9.10 DPI

DPI(Display Pixel Interface) 模块拥有 24 位并行数据线，由系统内存充当显存，通过持续输出数据和同步信号直接驱动屏幕显示，具有以下特性：

- 支持 16/18/24-bit 并行数据位宽
- 支持 YUV422/RGB565/RGB888/RGBA8888 输入格式
- 支持 RGB565/RGB666/RGB888 输出格式
- 支持单缓冲区和乒乓缓冲区作为显存
- 乒乓操作支持硬件或软件控制
- 支持测试模式（使用虚拟数据而非真实内存数据）

2.9.11 OSD

OSD(On-Screen Display) 模块用于实现画面图层的叠加，通过软件配置，可以将一个指定的图形叠加显示在底层图像之上。该模块具有以下特性：

- 一个 draw 模块，可以绘制 16 个不同风格 (颜色，边框宽度，填充、非填充) 的矩形
  - 矩形根据预定义的优先级确定显示 (覆盖) 的顺序
  - 矩形不支持透明度设置
- 两个 blend 模块，支持 2D 图层的混合 (叠加) 显示
  - 每个图层支持不同的像素格式，分成 RGB 及 YUV 两大类 (可配置颜色分量的排列顺序)，并支持硬件调色板
  - 每个图层可以使用全局颜色
  - 每个图层都能支持全局或像素级别 (某些颜色格式) 的 alpha 值，并支持图层间的 alpha blending
  - 每个图层依据不同的优先级确定显示 (覆盖) 的顺序
  - 每个图层均可支持 color keying

2.9.12 UART

芯片内置 4 个通用异步串行收发器 (UART0/1/2/3)，具有以下特性：

- 支持硬件的 CTS 和 RTS 流控
- 支持 LIN 主/从功能
- 可配置的数据位、停止位和奇偶校验位
- 支持普通/固定字符的自动波特率检测
- 工作时钟可以选择为 BCLK 、XCLK 或 160MHz，波特率最大支持 10Mbps
- TX 和 RX 具有独立 FIFO，FIFO 深度为 32 字节，支持 DMA 功能
- 支持 RTO 超时检测机制

2.9.13 I2C

芯片内置 3 个 I2C 接口，具有以下特性：

- 支持多主机模式和仲裁功能
- 工作时钟可以选择为 BCLK 或者 XCLK
- 支持标准模式（最大 100KHz）和快速模式（最大 400KHz），最快速度可达 1.8MHz（取决于外部上拉电阻的大小）
- 具有器件地址寄存器，寄存器地址寄存器，寄存器地址长度可设置为 1 字节/ 2 字节/ 3 字节/ 4 字节
- I2C 具有独立收发 FIFO，FIFO 深度为 2 word
- 支持 DMA 功能

2.9.14 SPI

芯片内置 4 个 SPI，可以配置为主机模式或者从机模式，SPI 模块时钟是 XCLK 或 160MHz，具有以下特性：

- 主机模式下，时钟频率最高为 40 MHz
- 从机模式下，允许主机最大的时钟频率为 40 MHz
- 每帧的位宽可以配置为 8 位/ 16 位/ 24 位/ 32 位
- 自适应的 FIFO 深度变化特性，适配高性能的场景应用
  - 当位宽为 32 位时，FIFO 的深度为 8

  - 当位宽为 24 位时，FIFO 的深度为 8
  - 当位宽为 16 位时，FIFO 的深度为 16
  - 当位宽为 8 位时，FIFO 的深度为 32
- 支持 DMA 传输模式

2.9.15 IPC

IPC(inter-processor communication) 是多核处理器之间通信的一种机制。

芯片具有两个 CPU 内核和 4 个 IPC 通道，有以下特点：

- 每个 IPC 通道都有独立的 32 位状态值
- 每个 IPC 通道都可以通过中断绑定到指定 CPU

2.9.16 TIMER

芯片内置 2 个 32-bit 通用定时器，每个定时器包含两个通道和 1 个看门狗定时器，具有以下特性：

- 通用定时器的时钟源可以选择 FCLK/32K/XTAL/GPIO，看门狗定时器的时钟源可以选择 FCLK/32K/XTAL/GPIO
- 每个计数器都有 8-bit 分频器
- 每组通用定时器都包含三个比较寄存器，支持比较中断，计数模式支持 FreeRun 模式和 PreLoad 模式
- 16-bit 看门狗定时器，支持中断或复位两种看门狗溢出方式

2.9.17 RTC

芯片内置一个 64-bit 的实时时钟计数器，具有以下特性：

- 支持低功耗模式下的唤醒
- 支持读取锁定，防止读取过程中被更新
- 支持阈值触发中断

2.9.18 GPADC

芯片内置两个 GPADC(ADC0/1)，具有以下特性：

- 最高采样率可达 2MHz

-总计 24 路外部通道输入，支持差分和单端输入-内置 PGA，放大增益 1~32 倍，6dB 一档-通过内置滤波器实现 14~16bit 数据输出-单次转换模式，连续转换模式，单次通道扫描，连续通道扫描，注入通道扫描等等

扫描模式-支持软件触发，GPIO 触发，PWM 触发和定时器触发-内置温度传感器 - 支持外部 1.25V 参考电压 - 最大可以测量 1.8V 外部输入电压

2.9.19 I2S

芯片内置一个 I2S 接口，具有以下特性：

- 支持主模式以及从模式
- 支持 Left-justified/ Right-justified/ DSP 等数据格式，数据宽度可配置为 8/16/24/32 比特
- 除单声道/双声道模式之外，同时支持四声道与六声道模式
- 支持播放单声道音频复制为双声道模式
- 支持动态静音切换功能
- I2S 具有独立收发 FIFO，FIFO 深度为 16 word
- 支持 DMA 功能

2.9.20 PWM

芯片内置 2 组 PWM 信号，每组包含 4 通道 PWM 信号输出，每通道可以设置为 2 路互补 PWM，具有以下特性：

- 三种时钟源 BCLK/XCLK/32K 可供选择，搭配 16-bit 时钟分频器
- 每组 PWM 都可以独立设置为不同的周期
- 每通道 PWM 都有双门限值设定，可以设定不同的占空比和相位，增加脉冲弹性
- 最快可产生频率为 40MHz 占空比为 50% 的方波，最慢可产生频率小于 1Hz 且占空比可调的波形
- 每通道 PWM 都有独立的死区时间设定
- 每路 PWM 输出引脚都可以设定不同的有效电平
- 每路 PWM 都有独立的连接开关用来选择是否与内部计数器相连，并可设定不连接时的默认输出电平
- 刹车信号可以将 PWM 输出电平置于预先设定的状态
- 多达 11 种可用于触发 ADC 转换的触发源
- 支持多种中断类型：计数器溢出中断、门限值比较中断、周期数中断

2.9.21 CANFD

芯片内置 3 个 CANFD，兼容 CAN2.0B，具有以下特性：

- 支持自定义位速率
- 支持标准帧和扩展帧
- 具有 6 帧的发送 FIFO 和 6 帧的接收 FIFO
- 支持自测模式（自发自收）
- 支持帧过滤功能，具有 16 个过滤器
- 支持静默模式（不应答，没有有效的错误标志）
- 支持不重发的单次传输
- 支持总线错误管理
- CANFD 支持时间触发的机制，兼容 ISO11898-4

2.9.22 KeyScan

KYS(KeyScan) 模块用于对矩阵键盘进行扫描以获取输入键值，具有以下特性：

- 行列数可配置，最大支持 8 行 *8 列的矩阵键盘扫描
- 支持 8 字节深度的键值 FIFO
- 扫描间隙可调
- 支持硬件消除噪声/毛刺功能
- 支持鬼键预测功能
- 支持扫描完成中断、FIFO 多种阈值中断和鬼键中断
- 支持低功耗唤醒

2.9.23 IR(IR-remote)

芯片内置一个红外遥控，具有以下特性：

- 时钟源为 XCLK，最高工作频率为 40MHz
- 支持发送和接收两种模式
- 发送在非自由模式下最多支持 65536-bit 数据位，自由模式下可连续发送任意长度数据

- 发送支持可配置的头/尾/逻辑 0/逻辑 1
- 发送支持可配置的载波频率和占空比
- 发送支持 DMA 模式
- 接收既支持以固定协议 NEC、RC-5 接收数据，也支持以脉冲宽度计数方式接收任意格式数据
- 接收最多支持 64-bit 数据位（固定协议方式），65535-bit 数据位（脉冲宽度计数方式）
- 接收 FIFO 深度为 128 字节（脉冲宽度计数方式）
- 发送和接收都支持 FIFO 阈值中断和完成中断

2.9.24 Audio ADC

BL618DG 集成 1 路音频 ADC（与高精度 ADC 不可同时使用），其特性如下：

- 采样率:8k~96k
- 信噪比 (A-W): 92dB @6dB 增益，48K 采样率
- 谐波失真 + 噪声: -88dB @6dB 增益，48K 采样率
- 模拟前置增益: 6~42 dB, 每档 3dB
- 模拟全差分输入
- 可调节的高通滤波器和数字音量控制
- 支持 PDM 接口（支持 1 路 DMIC）
- 输入信号复用 GPIO
- 32 位宽度的发送 FIFO，深度为 8
- 支持 DMA 传输模式

2.9.25 Audio DAC

BL618DG 集成 1 路音频 DAC，用于音频采集与播放场景，*BL618DG* 没有专用的音频 PLL ，Audio 模块的时钟来自 WiFi PLL 和 CPU PLL ，其特性如下：

- 采样率:8k~48k
- 信噪比 (A-W)：TBD 采样率
- 谐波失真 + 噪声：TBD 采样率

- 可调节的数字音量控制
- 支持差分互补输出
- 32 位宽度的发送 FIFO，深度为 16
- 支持 DMA 传输模式

（与 audio CODEC 不可同时使用）

2.9.26 Watchdog

BL618DG 内置数字看门狗和模拟看门狗，具有以下特性：

- 数字看门狗
  - 一个 16-bit Watchdog 定时器，工作在 active 模式
  - 支持写保护，防止误设定造成系统异常
  - 支持中断或复位两种方式
- 模拟看门狗
  - 一个基于 rtc 的 40-bit Watchdog 定时器，active 模式和低功耗模式下都能工作
  - 仅支持复位，不支持中断方式

2.9.27 Flash Controller

Flash 控制器支持 XIP（Execute In Place），允许代码直接从 Flash 执行，减少 RAM 占用。具备以下特性：

- 时钟源可以选择为 Wifipll 48M/80M/96M/120M、XTAL、BCLK
- Flash 频率最高可达 80 MHz
- 兼容 SPI、Dual SPI、Quad SPI 接口
- 支持 Flash 擦/读/写操作
- 支持硬件 XIP 解密，支持 AES CTR/XTS 模式
- 支持 Flash 24 位和 32 位地址模式
- 支持内封 Flash 和外置 Flash

2.9.28 Secure Boot

芯片支持 Secure Boot 功能，能够在启动过程中对 Bootloader 和应用程序固件进行验证，确保其完整性和可信性，从而有效防止未授权代码运行。具备以下特性：

- 签名验证：支持基于 SECP256R1 的签名验证
- 固件加密：支持 AES CTR/XTS 加密算法
- 防回滚保护：防止降级攻击，确保设备运行最新或指定版本的固件

2.9.29 SEC_ENG

SEC ENG 内置了多种运算模块，包括 AES、SHA、CRC、GMAC、PKA 和 TRNG。

- AES
  - 支持 128 位、192 位和 256 位密钥长度
  - 支持多种链接模式的加密和解密（ECB/CBC/CTR/XTS）
  - 密钥存储在 eFuse 中，带读写保护
  - 支持 AES LINK 功能
- SHA
  - 支持 SHA1/SHA224/SHA256/SHA384/SHA512
  - 支持 SHA LINK 功能
- TRNG
  - 单次生成 256 bits 随机数
  - 作为物理性随机数发生器工作
- CRC
  - 支持 CRC-32

2.9.30 DMA2D

BL618DG 内置 DMA2D 模块，具有以下特性：

- 2 组独立专用通道
- 可配置为 1D DMA 或 2D DMA 功能
- 独立控制来源与目标存取宽度 (单字节、双字节、四字节)
- 每个通道独立作为读写缓存
- 每个通道可被独立的外设硬件触发或是软件触发
- 支持外设包括 UART、I2C、SPI、DBI、DSI。
- 八种流程控制
  - DMA 流程控制，来源内存、目标内存
  - DMA 流程控制，来源内存、目标外设
  - DMA 流程控制，来源外设、目标内存
  - DMA 流程控制，来源外设、目标外设
  - 目标外设流程控制，来源外设、目标外设
  - 目标外设流程控制，来源内存、目标外设
  - 来源外设流程控制，来源外设、目标内存
  - 来源外设流程控制，来源外设、目标外设
- 支持 LLI 链表功能，提高 DMA 效率，每个节点可单独设置是否触发中断
- 以下特征为 2D DMA 特有：
  - 支持 8/16/32-bit 像素图形在任意方向上的平移
  - 支持 8/16/32-bit 像素图形 90/180/270 度旋转
  - 支持 8/16/32-bit 像素图形水平/垂直翻折
  - 支持 8/16/32-bit 像素图形填充
  - 支持 8/16/24/32-bit Color Key

2.9.31 MiPi-DSI

BL618DG 内置 MiPi-DSI 模块，具有以下特性：

- 支持 1-/2-/4-lane 模式
- 支持 RGB565/666/888 以及 YUV422 8-bit 格式
- 支持 Sync Event Mode 或 Sync Pulse Mode
- 支持 Escape Mode，且可搭配 DMA 功能使用

2.9.32 TOUCH

BL618DG 内置 1 组 touch 控制器，可在自扫描模式对最高 8 路通道扫描，互扫描模式对最高 16 个通道扫描。具备如下特性:

- 通道扫描时间可配置
- 支持触碰检测、触碰移除检测
- 扫描结果支持滤波处理，可降低毛刺信号影响
- 支持低功耗扫描模式
- 支持跳频模式，可降低同频干扰信号影响
- 触碰检测支持触碰时长可配置
- 支持自扫描模式及互扫描模式

3 管脚定义

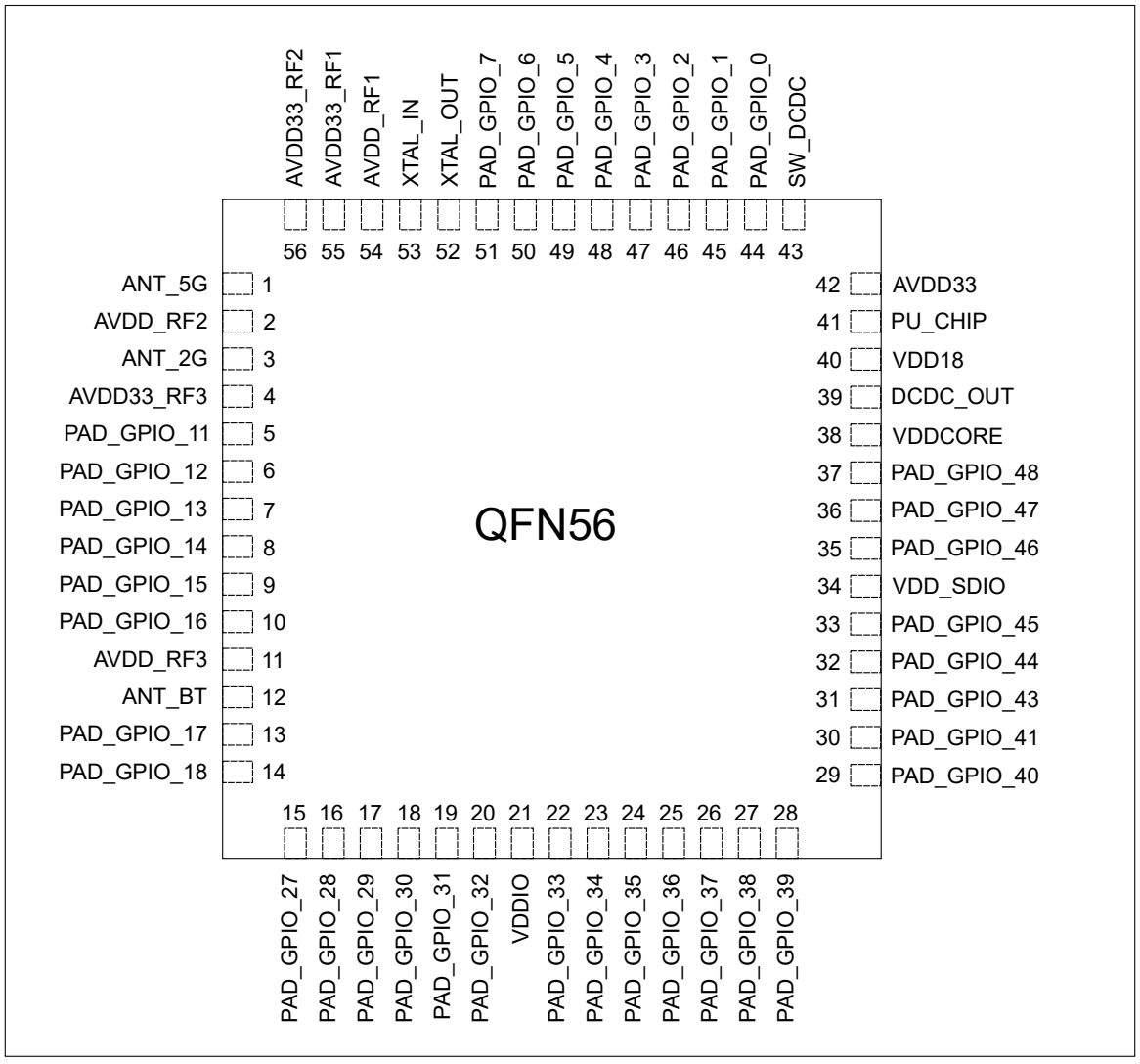

图 3.1: QFN56 管脚布局

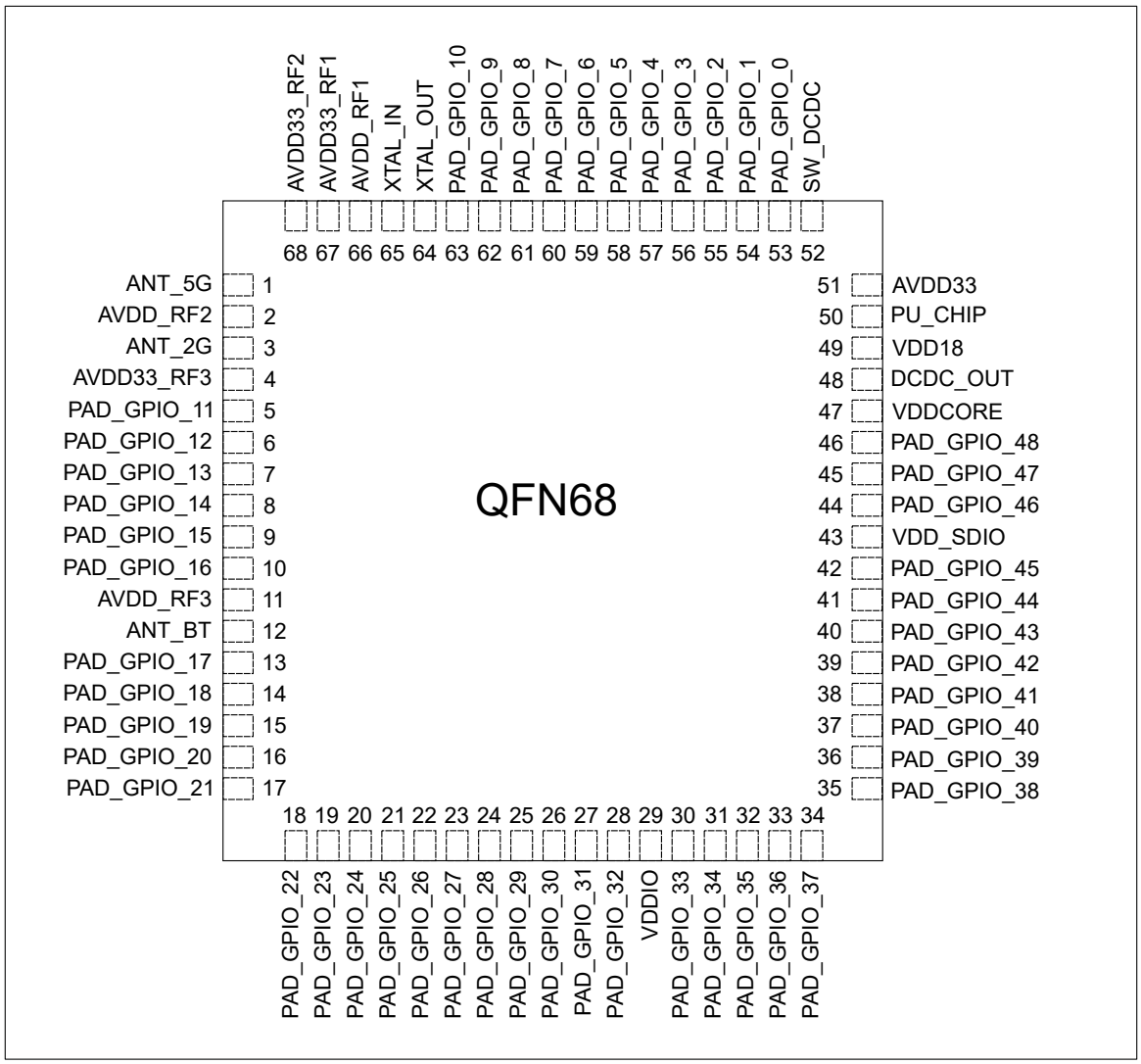

图 3.2: QFN68 管脚布局

表 3.1: 管脚定义

QFN56	QFN68	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
1	1		Analog	ANT_5G	-	-	-	-
2	2		Power,Input	AVDD_RF2	-	-	-	-
3	3		Analog	ANT_2G	-	-	-	-
4	4		Power,Input	AVDD33_RF3	-	-	-	-
5	5		DI/DO	PAD_GPIO_11	0	-	-	-
					1	-	SPI2_MOSI	SPI2 Master Output, Slave Input
					2	-	-	-
					3	-	I2S_DO/I2S_RCLK_O	I2S Data Output/I2S Receive Clock Output
					4	-	CANFD2_TX	CANFD2_TX
					5	-	I2C1_SCL	I2C 1 Serial Clock
					6	-	I2C2_SDA	I2C 2 Serial Data
					7	-	UART_SIG11	-
					8	-	-	-
					9	-	-	-
					10	-	ADC0_0/AUADC_0	-
					11	ir_rx_gpio_sel=0	SWGPIO[11]	Software GPIO 11
						ir_rx_gpio_sel=1	irrx	irrx
					12	-	-	-
					16	reg_pwm1_io_sel=0	pwm1_mc_out_c3p	PWM1 Channel 3 Positive
						reg_pwm1_io_sel=1	pwm2_mc_out_c1n	PWM2 Channel 1 Negative
					17	Signal Name	wl_jtag_tdi	WL JTAG Test Data Input
						Signal Name	-	-
					18	-	UART3_RXD	UART 3 Receive Data
					19	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					20	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
					21	-	AUDAC_PWM_P	AUDAC_PWM_P
					22	-	DBI_TypeB_WRn	Display Bus Interface Type B Write Control
					23	-	DBI_TypeC_SCL	Display Bus Interface Type C Serial Clock
					24	Signal Name	-	-
						Signal Name	-	-
					25	-	spdt_n	spdt_n
					26	-	main_jtag_tdi	MAIN_JTAG_TDI
					27	-	PEC_11	PEC_11
					28	-	rf_epa_gpio[3]	rf_epa_gpio[3]
					29	-	ant_switch_cntl[2]	ant_switch_cntl[2]
					30	Signal Name slave	-	-
						Signal Name master	-	-
					31	-	chip_clk_out[3]	-

表 3.1: 管脚定义 (continued)

QFN56	QFN68	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
6	6		DI/DO	PAD_GPIO_12	0	-	-	-
					1	-	SPI3_SS	SPI3 Slave Select
					2	-	-	-
					3	-	I2S_BCLK	I2S Bit Clock
					4	-	CANFD0_RX	CANFD0_RX
					5	-	I2C0_SDA	I2C 0 Serial Data
					6	-	I2C2_SCL	I2C 2 Serial Clock
					7	-	UART_SIG0 [1]	-
					8	-	-	-
					9	-	-	-
					10	-	ADC1_0/AUADC_1	-
					11	ir_rx_gpio_sel=0	SWGPIO[12]	Software GPIO 12
						ir_rx_gpio_sel=1	irrx	irrx
					12	-	-	-
					16	reg_pwm1_io_sel=0	pwm2_mc_out_c0p	PWM2 Channel 0 Positive
						reg_pwm1_io_sel=1	pwm2_mc_out_c2p	PWM2 Channel 2 Positive
					17	Signal Name	wl_jtag_tms/wl_cjtag_-tmsc	WL JTAG Test Mode Select/WL JTAG Test Mode Select and Control Counter
						Signal Name	ep_jtag_tms	EP JTAG Test Mode Select
					18	-	UART3_RTS	UART 3 Request To Send
					19	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					20	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
					21	-	AUDAC_PWM_N	AUDAC_PWM_N
					22	-	DBI_TypeB_CSn	Display Bus Interface Type B Chip Select
					23	-	DBI_TypeC_CSn	Display Bus Interface Type C Chip Select
					24	Signal Name	data0	-
						Signal Name	B0	-
					25	-	spdt_p	spdt_p
					26	-	main_jtag_tms/main_-cjtag_tmsc	MAIN_JTAG_TMS/MAIN JTAG Test Mode Select and Control Counter
					27	-	PEC_12	PEC_12
					28	-	rf_epa_gpio[4]	rf_epa_gpio[4]
					29	-	ant_switch_cntl[3]	ant_switch_cntl[3]
					30	Signal Name slave	epta_wl_act	epta_wl_act
						Signal Name master	epta_wl_act/gnt	epta_wl_act/gnt
					31	-	chip_clk_out[0]	-

表 3.1: 管脚定义 (continued)

QFN56	QFN68	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
7	7		DI/DO	PAD_GPIO_13	0	-	-	-
					1	-	SPI3_SCLK	SPI3 Serial Clock
					2	-	pdm_0_in	PDM Data Line
					3	-	I2S_FS	I2S Frame Sync
					4	-	CANFD0_TX	CANFD0_TX
					5	-	I2C0_SCL	I2C 0 Serial Clock
					6	-	I2C2_SDA	I2C 2 Serial Data
					7	-	UART_SIG1	-
					8	-	E1_MDIO	RMII Management Data Input/Output
					9	-	-	-
					10	-	ADC0_1/dc_tp_18/C_-EXT	-
					11	ir_rx_gpio_sel=0	SWGPIO[13]	Software GPIO 13
						ir_rx_gpio_sel=1	irrx	irrx
					12	-	-	-
					16	reg_pwm1_io_sel=0	pwm2_mc_out_c1p	PWM2 Channel 1 Positive
						reg_pwm1_io_sel=1	pwm2_mc_out_c2n	PWM2 Channel 2 Negative
					17	Signal Name	wl_jtag_tclk/wl_cjtag_tckc	WL JTAG Test Clock
						Signal Name	ep_jtag_tclk	EP JTAG Test Clock
					18	-	UART3_CTS	UART 3 Clear To Send
					19	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					20	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
					21	-	AUDAC_PWM_P	AUDAC_PWM_P
					22	-	DBI_TypeB_RDn	Display Bus Interface Type B Read Control
					23	-	DBI_TypeC_SDA0	Display Bus Interface Type C Serial Data 0
					24	Signal Name	data1	-
						Signal Name	B1	-
					25	-	spdt_n	spdt_n
					26	-	main_jtag_tck/main_-cjtag_tckc	MAIN_JTAG_TCK
					27	-	PEC_13	PEC_13
					28	-	rf_epa_gpio[5]	rf_epa_gpio[5]
					29	-	ant_switch_cntl[4]	ant_switch_cntl[4]
					30	Signal Name slave	epta_bl_act	epta_bl_act
						Signal Name master	epta_bl_act	epta_bl_act
					31	-	chip_clk_out[1]	-

表 3.1: 管脚定义 (continued)

QFN56	QFN68	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
8	8		DI/DO	PAD_GPIO_14	0	-	-	-
					1	-	SPI3_MISO	SPI3 Master Input, Slave Output
					2	-	pdm_clk_o	PDM Clock Line
					3	-	I2S_DI/I2S_RCLK_O	I2S Data Input/I2S Receive Clock Output
					4	-	CANFD1_RX	CANFD1_RX
					5	-	I2C1_SDA	I2C 1 Serial Data
					6	-	I2C2_SCL	I2C 2 Serial Clock
					7	-	UART_SIG2	-
					8	-	E1_MDC	RMII Management Data Clock
					9	-	-	-
					10	-	vref_ext[1]/touch_ch[2]	-
					11	ir_rx_gpio_sel=0	SWGPIO[14]	Software GPIO 14
						ir_rx_gpio_sel=1	irrx	irrx
					12	-	-	-
					16	reg_pwm1_io_sel=0	pwm2_mc_out_c2p	PWM2 Channel 2 Positive
						reg_pwm1_io_sel=1	pwm2_mc_out_c3p	PWM2 Channel 3 Positive
					17	Signal Name	wl_jtag_tdo	WL JTAG Test Data Out
						Signal Name	-	-
					18	-	UART3_TXD	UART 3 Transmit Data
					19	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					20	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
					21	-	AUDAC_PWM_N	AUDAC_PWM_N
					22	-	DBI_TypeB_DCn	Display Bus Interface Type B Data /Command Control
					23	-	DBI_TypeC_DCn	Display Bus Interface Type C Data /Command Control
					24	Signal Name	data2	-
						Signal Name	B2	-
					25	-	spdt_p	spdt_p
					26	-	main_jtag_tdo	MAIN_JTAG_TDO
					27	-	PEC_14	PEC_14
					28	-	rf_epa_gpio[6]	rf_epa_gpio[6]
					29	-	ant_switch_cntl[5]	ant_switch_cntl[5]
					30	Signal Name slave	epta_bt_pri	epta_bt_pri
						Signal Name master	epta_bt_pri	epta_bt_pri
					31	-	chip_clk_out[2]	-

表 3.1: 管脚定义 (continued)

QFN56	QFN68	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
9	9		DI/DO	PAD_GPIO_15	0	-	-	-
					1	-	SPI3_MOSI	SPI3 Master Output, Slave Input
					2	-	pdm_0_in	PDM Data Line
					3	-	I2S_DO/I2S_RCLK_O	I2S Data Output/I2S Receive Clock Output
					4	-	CANFD1_TX	CANFD1_TX
					5	-	I2C1_SCL	I2C 1 Serial Clock
					6	-	I2C2_SDA	I2C 2 Serial Data
					7	-	UART_SIG3	-
					8	-	-	-
					9	-	CAM0_DATA0	Camera Data 0
					10	-	ADC1_1/touch_ch[3]	-
					11	ir_rx_gpio_sel=0	SWGPIO[15]	Software GPIO 15
						ir_rx_gpio_sel=1	irrx	irrx
					12	-	-	-
					16	reg_pwm1_io_sel=0	pwm2_mc_out_c3p	PWM2 Channel 3 Positive
						reg_pwm1_io_sel=1	pwm2_mc_out_c3n	PWM2 Channel 3 Negative
					17	Signal Name	wl_jtag_tdi	WL JTAG Test Data Input
						Signal Name	-	-
					18	-	UART3_RXD	UART 3 Receive Data
					19	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					20	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
					21	-	-	-
					22	-	-	-
					23	-	-	-
					24	Signal Name	data3	-
						Signal Name	B3	-
					25	-	spdt_n	spdt_n
					26	-	main_jtag_tdi	MAIN_JTAG_TDI
					27	-	PEC_15	PEC_15
					28	-	rf_epa_gpio[7]	rf_epa_gpio[7]
					29	-	ant_switch_cntl[6]	ant_switch_cntl[6]
					30	Signal Name slave	-	-
						Signal Name master	-	-
					31	-	chip_clk_out[3]	-

表 3.1: 管脚定义 (continued)

QFN56	QFN68	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
10	10		DI/DO	PAD_GPIO_16	0	-	-	-
					1	-	SPI0_SS	SPI0 Slave Select
					2	-	pdm_clk_o	PDM Clock Line
					3	-	I2S_BCLK	I2S Bit Clock
					4	-	CANFD2_RX	CANFD2_RX
					5	-	I2C0_SDA	I2C 0 Serial Data
					6	-	I2C2_SCL	I2C 2 Serial Clock
					7	-	UART_SIG4	-
					8	-	E0_TX_EN	RMII Transmit Enable
					9	-	CAM0_DATA1	Camera Data 1
					10	-	ADC0_2/touch_ch[4]	-
					11	ir_rx_gpio_sel=0	SWGPIO[16]	Software GPIO 16
						ir_rx_gpio_sel=1	-	-
					12	-	-	-
					16	reg_pwm1_io_sel=0	pwm1_mc_out_c0p	PWM1 Channel 0 Positive
						reg_pwm1_io_sel=1	pwm1_mc_out_c0p	PWM1 Channel 0 Positive
					17	Signal Name	wl_jtag_tms/wl_cjtag_-tmsc	WL JTAG Test Mode Select/WL JTAG Test Mode Select and Control Counter
						Signal Name	ep_jtag_tms	EP JTAG Test Mode Select
					18	-	UART3_RTS	UART 3 Request To Send
					19	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					20	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
					21	-	AUDAC_PWM_P	AUDAC_PWM_P
					22	-	-	-
					23	-	-	-
					24	Signal Name	data4	-
						Signal Name	B4	-
					25	-	spdt_p	spdt_p
					26	-	main_jtag_tms/main_-cjtag_tmsc	MAIN_JTAG_TMS/MAIN JTAG Test Mode Select and Control Counter
					27	-	PEC_16	PEC_16
					28	-	rf_epa_gpio[0]	rf_epa_gpio[0]
					29	-	ant_switch_req	ant_switch_req
					30	Signal Name slave	epta_wl_act	epta_wl_act
						Signal Name master	epta_wl_act/gnt	epta_wl_act/gnt
					31	-	chip_clk_out[0]	-
11	11		Power,Input	AVDD_RF3	-	-	-	-
12	12		Analog	ANT_BT	-	-	-	-

表 3.1: 管脚定义 (continued)

QFN56	QFN68	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
13	13		DI/DO	PAD_GPIO_17	0	-	-	-
					1	-	SPI0_SCLK	SPI0 Serial Clock
					2	-	pdm_0_in	PDM Data Line
					3	-	I2S_FS	I2S Frame Sync
					4	-	CANFD2_TX	CANFD2_TX
					5	-	I2C0_SCL	I2C 0 Serial Clock
					6	-	I2C2_SDA	I2C 2 Serial Data
					7	-	UART_SIG5	-
					8	-	E0_MDIO	RMII Management Data Input/Output
					9	-	CAM0_DATA2	Camera Data 2
					10	-	ADC1_2/touch_ch[5]	-
					11	ir_rx_gpio_sel=0	SWGPIO[17]	Software GPIO 17
						ir_rx_gpio_sel=1	-	-
					12	-	-	-
					16	reg_pwm1_io_sel=0	pwm1_mc_out_c1p	PWM1 Channel 1 Positive
						reg_pwm1_io_sel=1	pwm1_mc_out_c0n	PWM1 Channel 0 Negative
					17	Signal Name	wl_jtag_tclk/wl_cjtag_tckc	WL JTAG Test Clock
						Signal Name	ep_jtag_tclk	EP JTAG Test Clock
					18	-	UART3_CTS	UART 3 Clear To Send
					19	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					20	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
					21	-	AUDAC_PWM_N	AUDAC_PWM_N
					22	-	DBI_TypeB_WRn	Display Bus Interface Type B Write Control
					23	-	-	-
					24	Signal Name	data5	-
						Signal Name	B5	-
					25	-	spdt_n	spdt_n
					26	-	main_jtag_tck/main_-cjtag_tckc	MAIN_JTAG_TCK
					27	-	PEC_17	PEC_17
					28	-	rf_epa_gpio[1]	rf_epa_gpio[1]
					29	-	ant_switch_cntl[0]	ant_switch_cntl[0]
					30	Signal Name slave	epta_bl_act	epta_bl_act
						Signal Name master	epta_bl_act	epta_bl_act
					31	-	chip_clk_out[1]	-

表 3.1: 管脚定义 (continued)

QFN56	QFN68	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
14	14		DI/DO	PAD_GPIO_18	0	-	-	-
					1	-	SPI0_MISO [2]	SPI0 Master Input, Slave Output
					2	-	pdm_clk_o	PDM Clock Line
					3	-	I2S_DI/I2S_RCLK_O	I2S Data Input/I2S Receive Clock Output
					4	-	CANFD0_RX	CANFD0_RX
					5	-	I2C1_SDA	I2C 1 Serial Data
					6	-	I2C2_SCL	I2C 2 Serial Clock
					7	-	UART_SIG6	-
					8	-	E0_MDC	RMII Management Data Clock
					9	-	CAM0_DATA3	Camera Data 3
					10	-	ADC0_3/touch_ch[6]	-
					11	ir_rx_gpio_sel=0	SWGPIO[18]	Software GPIO 18
						ir_rx_gpio_sel=1	-	-
					12	-	-	-
					16	reg_pwm1_io_sel=0	pwm1_mc_out_c2p	PWM1 Channel 2 Positive
						reg_pwm1_io_sel=1	pwm1_mc_out_c1p	PWM1 Channel 1 Positive
					17	Signal Name	wl_jtag_tdo	WL JTAG Test Data Out
						Signal Name	-	-
					18	-	UART3_TXD	UART 3 Transmit Data
					19	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					20	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
					21	-	AUDAC_PWM_P	AUDAC_PWM_P
					22	-	DBI_TypeB_CSn	Display Bus Interface Type B Chip Select
					23	-	-	-
					24	Signal Name	data6	-
						Signal Name	B6	-
					25	-	spdt_p	spdt_p
					26	-	main_jtag_tdo	MAIN_JTAG_TDO
					27	-	PEC_18	PEC_18
					28	-	rf_epa_gpio[2]	rf_epa_gpio[2]
					29	-	ant_switch_cntl[1]	ant_switch_cntl[1]
					30	Signal Name slave	epta_bt_pri	epta_bt_pri
						Signal Name master	epta_bt_pri	epta_bt_pri
					31	-	chip_clk_out[2]	-

表 3.1: 管脚定义 (continued)

QFN56	QFN68	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
-	15		DI/DO	PAD_GPIO_19	0	-	-	-
					1	-	SPI0_MOSI	SPI0 Master Output, Slave Input
					2	-	pdm_0_in	PDM Data Line
					3	-	I2S_DO/I2S_RCLK_O	I2S Data Output/I2S Receive Clock Output
					4	-	CANFD0_TX	CANFD0_TX
					5	-	I2C1_SCL	I2C 1 Serial Clock
					6	-	I2C2_SDA	I2C 2 Serial Data
					7	-	UART_SIG7	-
					8	-	-	-
					9	-	-	-
					10	-	AUADC_2/touch_ch[7]	-
					11	ir_rx_gpio_sel=0	SWGPIO[19]	Software GPIO 19
						ir_rx_gpio_sel=1	-	-
					12	-	-	-
					16	reg_pwm1_io_sel=0	pwm1_mc_out_c3p	PWM1 Channel 3 Positive
						reg_pwm1_io_sel=1	pwm1_mc_out_c1n	PWM1 Channel 1 Negative
					17	Signal Name	wl_jtag_tdi	WL JTAG Test Data Input
						Signal Name	-	-
					18	-	UART3_RXD	UART 3 Receive Data
					19	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					20	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
					21	-	AUDAC_PWM_N	AUDAC_PWM_N
					22	-	DBI_TypeB_RDn	Display Bus Interface Type B Read Control
					23	-	-	-
					24	Signal Name	data7	-
						Signal Name	B7	-
					25	-	spdt_n	spdt_n
					26	-	main_jtag_tdi	MAIN_JTAG_TDI
					27	-	PEC_19	PEC_19
					28	-	rf_epa_gpio[3]	rf_epa_gpio[3]
					29	-	ant_switch_cntl[2]	ant_switch_cntl[2]
					30	Signal Name slave	-	-
						Signal Name master	-	-
					31	-	chip_clk_out[3]	-

表 3.1: 管脚定义 (continued)

QFN56	QFN68	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
-	16		DI/DO	PAD_GPIO_20	0	-	-	-
					1	-	SPI1_SS	SPI1 Slave Select
					2	-	pdm_clk_o	PDM Clock Line
					3	-	I2S_BCLK	I2S Bit Clock
					4	-	CANFD1_RX	CANFD1_RX
					5	-	I2C0_SDA	I2C 0 Serial Data
					6	-	I2C2_SCL	I2C 2 Serial Clock
					7	-	UART_SIG8	-
					8	-	-	-
					9	-	-	-
					10	-	AUADC_3	-
					11	ir_rx_gpio_sel=0	SWGPIO[20]	Software GPIO 20
						ir_rx_gpio_sel=1	-	-
					12	-	-	-
					16	reg_pwm1_io_sel=0	pwm2_mc_out_c0p	PWM2 Channel 0 Positive
						reg_pwm1_io_sel=1	pwm1_mc_out_c2p	PWM1 Channel 2 Positive
					17	Signal Name	wl_jtag_tms/wl_cjtag_-tmsc	WL JTAG Test Mode Select/WL JTAG Test Mode Select and Control Counter
						Signal Name	ep_jtag_tms	EP JTAG Test Mode Select
					18	-	UART3_RTS	UART 3 Request To Send
					19	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					20	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
					21	-	AUDAC_PWM_P	AUDAC_PWM_P
					22	-	DBI_TypeB_DCn	Display Bus Interface Type B Data /Command Control
					23	-	-	-
					24	Signal Name	data8	-
						Signal Name	G0	-
					25	-	spdt_p	spdt_p
					26	-	main_jtag_tms/main_-cjtag_tmsc	MAIN_JTAG_TMS/MAIN JTAG Test Mode Select and Control Counter
					27	-	PEC_20	PEC_20
					28	-	rf_epa_gpio[4]	rf_epa_gpio[4]
					29	-	ant_switch_cntl[3]	ant_switch_cntl[3]
					30	Signal Name slave	epta_wl_act	epta_wl_act
						Signal Name master	epta_wl_act/gnt	epta_wl_act/gnt
					31	-	chip_clk_out[0]	-

表 3.1: 管脚定义 (continued)

QFN56	QFN68	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
-	17		DI/DO	PAD_GPIO_21	0	-	-	-
					1	-	SPI1_SCLK	SPI1 Serial Clock
					2	-	pdm_0_in	PDM Data Line
					3	-	I2S_FS	I2S Frame Sync
					4	-	CANFD1_TX	CANFD1_TX
					5	-	I2C0_SCL	I2C 0 Serial Clock
					6	-	I2C_SDA	I2C 2 Serial Data
					7	-	UART_SIG9	-
					8	-	-	-
					9	-	-	-
					10	-	-	-
					11	ir_rx_gpio_sel=0	SWGPIO[21]	Software GPIO 21
						ir_rx_gpio_sel=1	-	-
					12	-	-	-
					16	reg_pwm1_io_sel=0	pwm2_mc_out_c1p	PWM2 Channel 1 Positive
						reg_pwm1_io_sel=1	pwm1_mc_out_c2n	PWM1 Channel 2 Negative
					17	Signal Name	wl_jtag_tclk/wl_cjtag_tckc	WL JTAG Test Clock
						Signal Name	ep_jtag_tclk	EP JTAG Test Clock
					18	-	UART3_CTS	UART 3 Clear To Send
					19	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					20	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
					21	-	AUDAC_PWM_N	AUDAC_PWM_N
					22	-	DBI_TypeB_DB0	Display Bus Interface Type B Data Bit 0
					23	-	-	-
					24	Signal Name	data9	-
						Signal Name	G1	-
					25	-	spdt_n	spdt_n
					26	-	main_jtag_tck/main_-cjtag_tckc	MAIN_JTAG_TCK
					27	-	PEC_21	PEC_21
					28	-	rf_epa_gpio[5]	rf_epa_gpio[5]
					29	-	ant_switch_cntl[4]	ant_switch_cntl[4]
					30	Signal Name slave	epta_bl_act	epta_bl_act
						Signal Name master	epta_bl_act	epta_bl_act
					31	-	chip_clk_out[1]	-

表 3.1: 管脚定义 (continued)

QFN56	QFN68	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
-	18		DI/DO	PAD_GPIO_22	0	-	-	-
					1	-	SPI1_MISO	SPI1 Master Input, Slave Output
					2	-	pdm_clk_o	PDM Clock Line
					3	-	I2S_DI/I2S_RCLK_O	I2S Data Input/I2S Receive Clock Output
					4	-	CANFD2_RX	CANFD2_RX
					5	-	I2C1_SDA	I2C 1 Serial Data
					6	-	I2C2_SCL	I2C 2 Serial Clock
					7	-	UART_SIG10	-
					8	-	-	-
					9	-	-	-
					10	-	-	-
					11	ir_rx_gpio_sel=0	SWGPIO[22]	Software GPIO 22
						ir_rx_gpio_sel=1	-	-
					12	-	-	-
					16	reg_pwm1_io_sel=0	pwm2_mc_out_c2p	PWM2 Channel 2 Positive
						reg_pwm1_io_sel=1	pwm1_mc_out_c3p	PWM1 Channel 3 Positive
					17	Signal Name	wl_jtag_tdo	WL JTAG Test Data Out
						Signal Name	-	-
					18	-	UART3_TXD	UART 3 Transmit Data
					19	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					20	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
					21	-	AUDAC_PWM_P	AUDAC_PWM_P
					22	-	DBI_TypeB_DB1	Display Bus Interface Type B Data Bit 1
					23	-	-	-
					24	Signal Name	data10	-
						Signal Name	G2	-
					25	-	spdt_p	spdt_p
					26	-	main_jtag_tdo	MAIN_JTAG_TDO
					27	-	PEC_22	PEC_22
					28	-	rf_epa_gpio[6]	rf_epa_gpio[6]
					29	-	ant_switch_cntl[5]	ant_switch_cntl[5]
					30	Signal Name slave	epta_bt_pri	epta_bt_pri
						Signal Name master	epta_bt_pri	epta_bt_pri
					31	-	chip_clk_out[2]	-

表 3.1: 管脚定义 (continued)

QFN56	QFN68	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
-	19		DI/DO	PAD_GPIO_23	0	-	-	-
					1	-	SPI1_MOSI	SPI1 Master Output, Slave Input
					2	-	pdm_0_in	PDM Data Line
					3	-	I2S_DO/I2S_RCLK_O	I2S Data Output/I2S Receive Clock Output
					4	-	CANFD2_TX	CANFD2_TX
					5	-	I2C1_SCL	I2C 1 Serial Clock
					6	-	I2C2_SDA	I2C 2 Serial Data
					7	-	UART_SIG11	-
					8	-	-	-
					9	-	-	-
					10	-	dsi_dn0	-
					11	ir_rx_gpio_sel=0	SWGPIO[23]	Software GPIO 23
						ir_rx_gpio_sel=1	-	-
					12	-	-	-
					16	reg_pwm1_io_sel=0	pwm2_mc_out_c3p	PWM2 Channel 3 Positive
						reg_pwm1_io_sel=1	pwm1_mc_out_c3n	PWM1 Channel 3 Negative
					17	Signal Name	wl_jtag_tdi	WL JTAG Test Data Input
						Signal Name	-	-
					18	-	UART3_RXD	UART 3 Receive Data
					19	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					20	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
					21	-	AUDAC_PWM_N	AUDAC_PWM_N
					22	-	DBI_TypeB_DB2	Display Bus Interface Type B Data Bit 2
					23	-	-	-
					24	Signal Name	data11	-
						Signal Name	G3	-
					25	-	spdt_n	spdt_n
					26	-	main_jtag_tdi	MAIN_JTAG_TDI
					27	-	PEC_23	PEC_23
					28	-	rf_epa_gpio[7]	rf_epa_gpio[7]
					29	-	ant_switch_cntl[6]	ant_switch_cntl[6]
					30	Signal Name slave	-	-
						Signal Name master	-	-
					31	-	chip_clk_out[3]	-

表 3.1: 管脚定义 (continued)

QFN56	QFN68	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
-	20		DI/DO	PAD_GPIO_24	0	-	-	-
					1	-	SPI2_SS	SPI2 Slave Select
					2	-	pdm_clk_o	PDM Clock Line
					3	-	I2S_BCLK	I2S Bit Clock
					4	-	CANFD0_RX	CANFD0_RX
					5	-	I2C0_SDA	I2C 0 Serial Data
					6	-	I2C2_SCL	I2C 2 Serial Clock
					7	-	UART_SIG0	-
					8	-	-	-
					9	-	-	-
					10	-	dsi_dp0	-
					11	ir_rx_gpio_sel=0	SWGPIO[24]	Software GPIO 24
						ir_rx_gpio_sel=1	-	-
					12	-	-	-
					16	reg_pwm1_io_sel=0	pwm1_mc_out_c0p	PWM1 Channel 0 Positive
						reg_pwm1_io_sel=1	pwm2_mc_out_c0p	PWM2 Channel 0 Positive
					17	Signal Name	wl_jtag_tms/wl_cjtag_-tmsc	WL JTAG Test Mode Select/WL JTAG Test Mode Select and Control Counter
						Signal Name	ep_jtag_tms	EP JTAG Test Mode Select
					18	-	UART3_RTS	UART 3 Request To Send
					19	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					20	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
					21	-	AUDAC_PWM_P	AUDAC_PWM_P
					22	-	DBI_TypeB_DB3	Display Bus Interface Type B Data Bit 3
					23	-	-	-
					24	Signal Name	data12	-
						Signal Name	G4	-
					25	-	spdt_p	spdt_p
					26	-	main_jtag_tms/main_-cjtag_tmsc	MAIN_JTAG_TMS/MAIN JTAG Test Mode Select and Control Counter
					27	-	PEC_24	PEC_24
					28	-	rf_epa_gpio[0]	rf_epa_gpio[0]
					29	-	ant_switch_req	ant_switch_req
					30	Signal Name slave	epta_wl_act	epta_wl_act
						Signal Name master	epta_wl_act/gnt	epta_wl_act/gnt
					31	-	chip_clk_out[0]	-

表 3.1: 管脚定义 (continued)

QFN56	QFN68	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
-	21		DI/DO	PAD_GPIO_25	0	-	-	-
					1	-	SPI2_SCLK	SPI2 Serial Clock
					2	-	pdm_0_in	PDM Data Line
					3	-	I2S_FS	I2S Frame Sync
					4	-	CANFD0_TX	CANFD0_TX
					5	-	I2C0_SCL	I2C 0 Serial Clock
					6	-	I2C2_SDA	I2C 2 Serial Data
					7	-	UART_SIG1	-
					8	-	-	-
					9	-	-	-
					10	-	ADC1_5/dsi_dn1	-
					11	ir_rx_gpio_sel=0	SWGPIO[25]	Software GPIO 25
						ir_rx_gpio_sel=1	-	-
					12	-	-	-
					16	reg_pwm1_io_sel=0	pwm1_mc_out_c1p	PWM1 Channel 1 Positive
						reg_pwm1_io_sel=1	pwm2_mc_out_c0n	PWM2 Channel 0 Negative
					17	Signal Name	wl_jtag_tclk/wl_cjtag_tckc	WL JTAG Test Clock
						Signal Name	ep_jtag_tclk	EP JTAG Test Clock
					18	-	UART3_CTS	UART 3 Clear To Send
					19	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					20	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
					21	-	AUDAC_PWM_N	AUDAC_PWM_N
					22	-	DBI_TypeB_DB4	Display Bus Interface Type B Data Bit 4
					23	-	-	-
					24	Signal Name	data13	-
						Signal Name	G5	-
					25	-	spdt_n	spdt_n
					26	-	main_jtag_tck/main_-cjtag_tckc	MAIN_JTAG_TCK
					27	-	PEC_25	PEC_25
					28	-	rf_epa_gpio[1]	rf_epa_gpio[1]
					29	-	ant_switch_cntl[0]	ant_switch_cntl[0]
					30	Signal Name slave	epta_bl_act	epta_bl_act
						Signal Name master	epta_bl_act	epta_bl_act
					31	-	chip_clk_out[1]	-

表 3.1: 管脚定义 (continued)

QFN56	QFN68	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
-	22		DI/DO	PAD_GPIO_26	0	-	-	-
					1	-	SPI2_MISO	SPI2 Master Input, Slave Output
					2	-	pdm_clk_o	PDM Clock Line
					3	-	I2S_DI/I2S_RCLK_O	I2S Data Input/I2S Receive Clock Output
					4	-	CANFD1_RX	CANFD1_RX
					5	-	I2C1_SDA	I2C 1 Serial Data
					6	-	I2C2_SCL	I2C 2 Serial Clock
					7	-	UART_SIG2	-
					8	-	-	-
					9	-	-	-
					10	-	ADC0_11/dsi_dp1	-
					11	ir_rx_gpio_sel=0	SWGPIO[26]	Software GPIO 26
						ir_rx_gpio_sel=1	-	-
					12	-	-	-
					16	reg_pwm1_io_sel=0	pwm1_mc_out_c2p	PWM1 Channel 2 Positive
						reg_pwm1_io_sel=1	pwm2_mc_out_c1p	PWM2 Channel 1 Positive
					17	Signal Name	wl_jtag_tdo	WL JTAG Test Data Out
						Signal Name	-	-
					18	-	UART3_TXD	UART 3 Transmit Data
					19	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					20	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
					21	-	AUDAC_PWM_P	AUDAC_PWM_P
					22	-	DBI_TypeB_DB5	Display Bus Interface Type B Data Bit 5
					23	-	-	-
					24	Signal Name	data14	-
						Signal Name	G6	-
					25	-	spdt_p	spdt_p
					26	-	main_jtag_tdo	MAIN_JTAG_TDO
					27	-	PEC_26	PEC_26
					28	-	rf_epa_gpio[2]	rf_epa_gpio[2]
					29	-	ant_switch_cntl[1]	ant_switch_cntl[1]
					30	Signal Name slave	epta_bt_pri	epta_bt_pri
						Signal Name master	epta_bt_pri	epta_bt_pri
					31	-	chip_clk_out[2]	-

表 3.1: 管脚定义 (continued)

QFN56	QFN68	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
15	23		DI/DO	PAD_GPIO_27	0	-	-	-
					1	-	SPI2_MOSI	SPI2 Master Output, Slave Input
					2	-	pdm_0_in	PDM Data Line
					3	-	I2S_DO/I2S_RCLK_O	I2S Data Output/I2S Receive Clock Output
					4	-	CANFD1_TX	CANFD1_TX
					5	-	I2C1_SCL	I2C 1 Serial Clock
					6	-	I2C2_SDA	I2C 2 Serial Data
					7	-	UART_SIG3	-
					8	-	E0_REF_CLK	RMII Reference Clock
					9	-	CAM0_HSYNC	Camera Horizontal Sync
					10	-	ADC1_11/dsi_dn_clk	-
					11	ir_rx_gpio_sel=0	SWGPIO[27]	Software GPIO 27
						ir_rx_gpio_sel=1	-	-
					12	-	-	-
					16	reg_pwm1_io_sel=0	pwm1_mc_out_c3p	PWM1 Channel 3 Positive
						reg_pwm1_io_sel=1	pwm2_mc_out_c1n	PWM2 Channel 1 Negative
					17	Signal Name	wl_jtag_tdi	WL JTAG Test Data Input
						Signal Name	-	-
					18	-	UART3_RXD	UART 3 Receive Data
					19	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					20	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
					21	-	AUDAC_PWM_N	AUDAC_PWM_N
					22	-	DBI_TypeB_DB6	Display Bus Interface Type B Data Bit 6
					23	-	-	-
					24	Signal Name	data15	-
						Signal Name	G7	-
					25	-	spdt_n	spdt_n
					26	-	main_jtag_tdi	MAIN_JTAG_TDI
					27	-	PEC_27	PEC_27
					28	-	rf_epa_gpio[3]	rf_epa_gpio[3]
					29	-	ant_switch_cntl[2]	ant_switch_cntl[2]
					30	Signal Name slave	-	-
						Signal Name master	-	-
					31	-	chip_clk_out[3]	-

表 3.1: 管脚定义 (continued)

QFN56	QFN68	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
16	24		DI/DO	PAD_GPIO_28	0	-	-	-
					1	-	SPI3_SS	SPI3 Slave Select
					2	-	pdm_clk_o	PDM Clock Line
					3	-	I2S_BCLK	I2S Bit Clock
					4	-	CANFD2_RX	CANFD2_RX
					5	-	I2C0_SDA	I2C 0 Serial Data
					6	-	I2C2_SCL	I2C 2 Serial Clock
					7	-	UART_SIG4	-
					8	-	E0_TXD[0]	RMII Transmit Data[0]
					9	-	CAM0_VSYNC	Camera Vertical Sync
					10	-	ADC1_3/dsi_dp_clk	-
					11	ir_rx_gpio_sel=0	SWGPIO[28]	Software GPIO 28
						ir_rx_gpio_sel=1	-	-
					12	-	-	-
					16	reg_pwm1_io_sel=0	pwm2_mc_out_c0p	PWM2 Channel 0 Positive
						reg_pwm1_io_sel=1	pwm2_mc_out_c2p	PWM2 Channel 2 Positive
					17	Signal Name	wl_jtag_tms/wl_cjtag_-tmsc	WL JTAG Test Mode Select/WL JTAG Test Mode Select and Control Counter
						Signal Name	ep_jtag_tms	EP JTAG Test Mode Select
					18	-	UART3_RTS	UART 3 Request To Send
					19	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					20	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
					21	-	AUDAC_PWM_P	AUDAC_PWM_P
					22	-	DBI_TypeB_DB7	Display Bus Interface Type B Data Bit 7
					23	-	-	-
					24	Signal Name	data16	-
						Signal Name	R0	-
					25	-	spdt_p	spdt_p
					26	-	main_jtag_tms/main_-cjtag_tmsc	MAIN_JTAG_TMS/MAIN JTAG Test Mode Select and Control Counter
					27	-	PEC_28	PEC_28
					28	-	rf_epa_gpio[4]	rf_epa_gpio[4]
					29	-	ant_switch_cntl[3]	ant_switch_cntl[3]
					30	Signal Name slave	epta_wl_act	epta_wl_act
						Signal Name master	epta_wl_act/gnt	epta_wl_act/gnt
					31	-	chip_clk_out[0]	-

表 3.1: 管脚定义 (continued)

QFN56	QFN68	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
17	25		DI/DO	PAD_GPIO_29	0	-	-	-
					1	-	SPI3_SCLK	SPI3 Serial Clock
					2	-	pdm_0_in	PDM Data Line
					3	-	I2S_FS	I2S Frame Sync
					4	-	CANFD2_TX	CANFD2_TX
					5	-	I2C0_SCL	I2C 0 Serial Clock
					6	-	I2C2_SDA	I2C 2 Serial Data
					7	-	UART_SIG5	-
					8	-	E0_TXD[1]	RMII Transmit Data[1]
					9	-	CAM0_CLK	Camera Clock
					10	-	ADC0_4/dsi_dn2	-
					11	ir_rx_gpio_sel=0	SWGPIO[29]	Software GPIO 29
						ir_rx_gpio_sel=1	-	-
					12	-	-	-
					16	reg_pwm1_io_sel=0	pwm2_mc_out_c1p	PWM2 Channel 1 Positive
						reg_pwm1_io_sel=1	pwm2_mc_out_c2n	PWM2 Channel 2 Negative
					17	Signal Name	wl_jtag_tclk/wl_cjtag_tckc	WL JTAG Test Clock
						Signal Name	ep_jtag_tclk	EP JTAG Test Clock
					18	-	UART3_CTS	UART 3 Clear To Send
					19	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					20	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
					21	-	AUDAC_PWM_N	AUDAC_PWM_N
					22	-	-	-
					23	-	-	-
					24	Signal Name	data17	-
						Signal Name	R1	-
					25	-	spdt_n	spdt_n
					26	-	main_jtag_tck/main_-cjtag_tckc	MAIN_JTAG_TCK
					27	-	PEC_29	PEC_29
					28	-	rf_epa_gpio[5]	rf_epa_gpio[5]
					29	-	ant_switch_cntl[4]	ant_switch_cntl[4]
					30	Signal Name slave	epta_bl_act	epta_bl_act
						Signal Name master	epta_bl_act	epta_bl_act
					31	-	chip_clk_out[1]	-

表 3.1: 管脚定义 (continued)

QFN56	QFN68	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
18	26		DI/DO	PAD_GPIO_30	0	-	-	-
					1	-	SPI3_MISO	SPI3 Master Input, Slave Output
					2	-	pdm_clk_o	PDM Clock Line
					3	-	I2S_DI/I2S_RCLK_O	I2S Data Input/I2S Receive Clock Output
					4	-	CANFD0_RX	CANFD0_RX
					5	-	I2C1_SDA	I2C 1 Serial Data
					6	-	I2C2_SCL	I2C 2 Serial Clock
					7	-	UART_SIG6	-
					8	-	E0_RXD[0]	RMII Receive Data[0]
					9	-	CAM0_DATA4	Camera Data 4
					10	-	ADC1_4/AUADC_4/dsi_-dp2	-
					11	ir_rx_gpio_sel=0	SWGPIO[30]	Software GPIO 30
						ir_rx_gpio_sel=1	irrx	irrx
					12	-	-	-
					16	reg_pwm1_io_sel=0	pwm2_mc_out_c2p	PWM2 Channel 2 Positive
						reg_pwm1_io_sel=1	pwm2_mc_out_c3p	PWM2 Channel 3 Positive
					17	Signal Name	wl_jtag_tdo	WL JTAG Test Data Out
						Signal Name	-	-
					18	-	UART3_TXD	UART 3 Transmit Data
					19	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					20	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
					21	-	-	-
					22	-	-	-
					23	-	-	-
					24	Signal Name	data18	-
						Signal Name	R2	-
					25	-	spdt_p	spdt_p
					26	-	main_jtag_tdo	MAIN_JTAG_TDO
					27	-	PEC_30	PEC_30
					28	-	rf_epa_gpio[6]	rf_epa_gpio[6]
					29	-	ant_switch_cntl[5]	ant_switch_cntl[5]
					30	Signal Name slave	epta_bt_pri	epta_bt_pri
						Signal Name master	epta_bt_pri	epta_bt_pri
					31	-	chip_clk_out[2]	-

表 3.1: 管脚定义 (continued)

QFN56	QFN68	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
19	27		DI/DO	PAD_GPIO_31	0	-	-	-
					1	-	SPI3_MOSI	SPI3 Master Output, Slave Input
					2	-	pdm_0_in	PDM Data Line
					3	-	I2S_DO/I2S_RCLK_O	I2S Data Output/I2S Receive Clock Output
					4	-	CANFD0_TX	CANFD0_TX
					5	-	I2C1_SCL	I2C 1 Serial Clock
					6	-	I2C2_SDA	I2C 2 Serial Data
					7	-	UART_SIG7	-
					8	-	E0_RXD[1]	RMII Receive Data[1]
					9	-	CAM0_DATA5	Camera Data 5
					10	-	ADC0_5/AUADC_5/dsi_-dn3	-
					11	ir_rx_gpio_sel=0	SWGPIO[31]	Software GPIO 31
						ir_rx_gpio_sel=1	irrx	irrx
					12	-	-	-
					16	reg_pwm1_io_sel=0	pwm2_mc_out_c3p	PWM2 Channel 3 Positive
						reg_pwm1_io_sel=1	pwm2_mc_out_c3n	PWM2 Channel 3 Negative
					17	Signal Name	wl_jtag_tdi	WL JTAG Test Data Input
						Signal Name	-	-
					18	-	UART3_RXD	UART 3 Receive Data
					19	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					20	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
					21	-	AUDAC_PWM_P	AUDAC_PWM_P
					22	-	-	-
					23	-	-	-
					24	Signal Name	data19	-
						Signal Name	R3	-
					25	-	spdt_n	spdt_n
					26	-	main_jtag_tdi	MAIN_JTAG_TDI
					27	-	PEC_31	PEC_31
					28	-	rf_epa_gpio[7]	rf_epa_gpio[7]
					29	-	ant_switch_cntl[6]	ant_switch_cntl[6]
					30	Signal Name slave	-	-
						Signal Name master	-	-
					31	-	chip_clk_out[3]	-

表 3.1: 管脚定义 (continued)

QFN56	QFN68	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
20	28		DI/DO	PAD_GPIO_32	0	-	-	-
					1	-	SPI0_SS	SPI0 Slave Select
					2	-	pdm_clk_o	PDM Clock Line
					3	-	I2S_BCLK	I2S Bit Clock
					4	-	CANFD1_RX	CANFD1_RX
					5	-	I2C0_SDA	I2C 0 Serial Data
					6	-	I2C2_SCL	I2C 2 Serial Clock
					7	-	UART_SIG8	-
					8	-	E0_RX_DV	RMII Receive Data Valid
					9	-	CAM0_DATA6	Camera Data 6
					10	-	vref_ext[2]/dsi_dp3	-
					11	ir_rx_gpio_sel=0	SWGPIO[32]	Software GPIO 32
						ir_rx_gpio_sel=1	irrx	irrx
					12	-	-	-
					16	reg_pwm1_io_sel=0	pwm1_mc_out_c0p	PWM1 Channel 0 Positive
						reg_pwm1_io_sel=1	pwm1_mc_out_c2p	PWM1 Channel 0 Positive
					17	Signal Name	wl_jtag_tms/wl_cjtag_-tmsc	WL JTAG Test Mode Select/WL JTAG Test Mode Select and Control Counter
						Signal Name	ep_jtag_tms	EP JTAG Test Mode Select
					18	-	UART3_RTS	UART 3 Request To Send
					19	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					20	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
					21	-	AUDAC_PWM_N	AUDAC_PWM_N
					22	-	-	-
					23	-	-	-
					24	Signal Name	data20	-
						Signal Name	R4	-
					25	-	spdt_p	spdt_p
					26	-	main_jtag_tms/main_-cjtag_tmsc	MAIN_JTAG_TMS/MAIN JTAG Test Mode Select and Control Counter
					27	-	PEC_32	PEC_32
					28	-	rf_epa_gpio[0]	rf_epa_gpio[0]
					29	-	ant_switch_req	ant_switch_req
					30	Signal Name slave	epta_wl_act	epta_wl_act
						Signal Name master	epta_wl_act/gnt	epta_wl_act/gnt
					31	-	chip_clk_out[0]	-
21	29			VDDIO	-	-	-	-

表 3.1: 管脚定义 (continued)

QFN56	QFN68	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
22	30		DI/DO	PAD_GPIO_33	0	-	-	-
					1	-	SPI0_SCLK	SPI0 Serial Clock
					2	-	-	-
					3	-	I2S_FS	I2S Frame Sync
					4	-	CANFD1_TX	CANFD1_TX
					5	-	I2C0_SCL	I2C 0 Serial Clock
					6	-	I2C2_SDA	I2C 2 Serial Data
					7	-	UART_SIG9	-
					8	-	E0_RX_ERR	-
					9	-	CAM0_DATA7	Camera Data 7
					10	-	-	-
					11	ir_rx_gpio_sel=0	SWGPIO[33]	Software GPIO 33
						ir_rx_gpio_sel=1	-	-
					12	-	-	-
					16	reg_pwm1_io_sel=0	pwm1_mc_out_c1p	PWM1 Channel 1 Positive
						reg_pwm1_io_sel=1	pwm1_mc_out_c2n	PWM1 Channel 0 Negative
					17	Signal Name	wl_jtag_tclk/wl_cjtag_tckc	WL JTAG Test Clock
						Signal Name	ep_jtag_tclk	EP JTAG Test Clock
					18	-	UART3_CTS	UART 3 Clear To Send
					19	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					20	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
					21	-	AUDAC_PWM_P	AUDAC_PWM_P
					22	-	-	-
					23	-	-	-
					24	Signal Name	data21	-
						Signal Name	R5	-
					25	-	spdt_n	spdt_n
					26	-	main_jtag_tck/main_-cjtag_tckc	MAIN_JTAG_TCK
					27	-	PEC_33	PEC_33
					28	-	rf_epa_gpio[1]	rf_epa_gpio[1]
					29	-	ant_switch_cntl[0]	ant_switch_cntl[0]
					30	Signal Name slave	epta_bl_act	epta_bl_act
						Signal Name master	epta_bl_act	epta_bl_act
					31	-	chip_clk_out[1]	-

表 3.1: 管脚定义 (continued)

QFN56	QFN68	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
23	31		DI/DO	PAD_GPIO_34	0	-	Data2	SD Host Data 2
					1	-	SPI0_MISO	SPI0 Master Input, Slave Output
					2	-	SFlash_CS [3]	NOR FALSH controller signal2 Chip Select
					3	-	I2S_DI/I2S_RCLK_O	I2S Data Input/I2S Receive Clock Output
					4	-	CANFD2_RX	CANFD2_RX
					5	-	I2C1_SDA	I2C 1 Serial Data
					6	-	I2C2_SCL	I2C 2 Serial Clock
					7	-	UART_SIG10	-
					8	-	-	-
					9	-	-	-
					10	-	-	-
					11	ir_rx_gpio_sel=0	SWGPIO[34]	Software GPIO 34
						ir_rx_gpio_sel=1	-	-
					12	-	SDIO_DAT2	SDIO_DAT2
					16	reg_pwm1_io_sel=0	pwm1_mc_out_c2p	PWM1 Channel 2 Positive
						reg_pwm1_io_sel=1	pwm1_mc_out_c3p	PWM1 Channel 1 Positive
					17	Signal Name	wl_jtag_tdo	WL JTAG Test Data Out
						Signal Name	-	-
					18	-	UART3_TXD	UART 3 Transmit Data
					19	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					20	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
					21	-	-	-
					22	-	-	-
					23	-	-	-
					24	Signal Name	-	-
						Signal Name	-	-
					25	-	spdt_p	spdt_p
					26	-	main_jtag_tdo	MAIN_JTAG_TDO
					27	-	PEC_34	PEC_34
					28	-	rf_epa_gpio[2]	rf_epa_gpio[2]
					29	-	ant_switch_cntl[1]	ant_switch_cntl[1]
					30	Signal Name slave	epta_bt_pri	epta_bt_pri
						Signal Name master	epta_bt_pri	epta_bt_pri
					31	-	chip_clk_out[2]	-

表 3.1: 管脚定义 (continued)

QFN56	QFN68	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
24	32		DI/DO	PAD_GPIO_35	0	-	Data3	SD Host Data 3
					1	-	SPI0_MOSI	SPI0 Master Output, Slave Input
					2	-	SFlash_D0	NOR FALSH controller signal2 Data 0
					3	-	I2S_DO/I2S_RCLK_O	I2S Data Output/I2S Receive Clock Output
					4	-	CANFD2_TX	CANFD2_TX
					5	-	I2C1_SCL	I2C 1 Serial Clock
					6	-	I2C2_SDA	I2C 2 Serial Data
					7	-	UART_SIG11	-
					8	-	-	-
					9	-	-	-
					10	-	-	-
					11	ir_rx_gpio_sel=0	SWGPIO[35]	Software GPIO 35
						ir_rx_gpio_sel=1	-	-
					12	-	SDIO_DAT3	SDIO_DAT3
					16	reg_pwm1_io_sel=0	pwm1_mc_out_c3p	PWM1 Channel 3 Positive
						reg_pwm1_io_sel=1	pwm1_mc_out_c3n	PWM1 Channel 1 Negative
					17	Signal Name	wl_jtag_tdi	WL JTAG Test Data Input
						Signal Name	-	-
					18	-	UART3_RXD	UART 3 Receive Data
					19	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					20	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
					21	-	-	-
					22	-	-	-
					23	-	-	-
					24	Signal Name	-	-
						Signal Name	-	-
					25	-	spdt_n	spdt_n
					26	-	main_jtag_tdi	MAIN_JTAG_TDI
					27	-	PEC_35	PEC_35
					28	-	rf_epa_gpio[3]	rf_epa_gpio[3]
					29	-	ant_switch_cntl[2]	ant_switch_cntl[2]
					30	Signal Name slave	-	-
						Signal Name master	-	-
					31	-	chip_clk_out[3]	-

表 3.1: 管脚定义 (continued)

QFN56	QFN68	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
25	33		DI/DO	PAD_GPIO_36	0	-	CMD	SD Host Command
					1	-	SPI1_SS	SPI1 Slave Select
					2	-	SFlash_D1	NOR FALSH controller signal2 Data 1
					3	-	I2S_BCLK	I2S Bit Clock
					4	-	CANFD0_RX	CANFD0_RX
					5	-	I2C0_SDA	I2C 0 Serial Data
					6	-	I2C2_SCL	I2C 2 Serial Clock
					7	-	UART_SIG0	-
					8	-	-	-
					9	-	-	-
					10	-	-	-
					11	ir_rx_gpio_sel=0	SWGPIO[36]	Software GPIO 36
						ir_rx_gpio_sel=1	-	-
					12	-	SDIO_CMD	SDIO_CMD
					16	reg_pwm1_io_sel=0	pwm2_mc_out_c0p	PWM2 Channel 0 Positive
						reg_pwm1_io_sel=1	pwm1_mc_out_c2p	PWM1 Channel 2 Positive
					17	Signal Name	wl_jtag_tms/wl_cjtag_-tmsc	WL JTAG Test Mode Select/WL JTAG Test Mode Select and Control Counter
						Signal Name	ep_jtag_tms	EP JTAG Test Mode Select
					18	-	UART3_RTS	UART 3 Request To Send
					19	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					20	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
					21	-	-	-
					22	-	-	-
					23	-	-	-
					24	Signal Name	-	-
						Signal Name	-	-
					25	-	spdt_p	spdt_p
					26	-	main_jtag_tms/main_-cjtag_tmsc	MAIN_JTAG_TMS/MAIN JTAG Test Mode Select and Control Counter
					27	-	PEC_36	PEC_36
					28	-	rf_epa_gpio[4]	rf_epa_gpio[4]
					29	-	ant_switch_cntl[3]	ant_switch_cntl[3]
					30	Signal Name slave	epta_wl_act	epta_wl_act
						Signal Name master	epta_wl_act/gnt	epta_wl_act/gnt
					31	-	chip_clk_out[0]	-

表 3.1: 管脚定义 (continued)

QFN56	QFN68	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
26	34		DI/DO	PAD_GPIO_37	0	-	CLK	SD Host Clock
					1	-	SPI1_SCLK	SPI1 Serial Clock
					2	-	SFlash_D2	NOR FALSH controller signal2 Data 2
					3	-	I2S_FS	I2S Frame Sync
					4	-	CANFD0_TX	CANFD0_TX
					5	-	I2C0_SCL	I2C 0 Serial Clock
					6	-	I2C2_SDA	I2C 2 Serial Data
					7	-	UART_SIG1	-
					8	-	-	-
					9	-	-	-
					10	-	-	-
					11	ir_rx_gpio_sel=0	SWGPIO[37]	Software GPIO 37
						ir_rx_gpio_sel=1	-	-
					12	-	SDIO_CLK	SDIO_CLK
					16	reg_pwm1_io_sel=0	pwm2_mc_out_c1p	PWM2 Channel 1 Positive
						reg_pwm1_io_sel=1	pwm1_mc_out_c2n	PWM1 Channel 2 Negative
					17	Signal Name	wl_jtag_tclk/wl_cjtag_tckc	WL JTAG Test Clock
						Signal Name	ep_jtag_tclk	EP JTAG Test Clock
					18	-	UART3_CTS	UART 3 Clear To Send
					19	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					20	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
					21	-	-	-
					22	-	-	-
					23	-	-	-
					24	Signal Name	-	-
						Signal Name	-	-
					25	-	spdt_n	spdt_n
					26	-	main_jtag_tck/main_-cjtag_tckc	MAIN_JTAG_TCK
					27	-	PEC_37	PEC_37
					28	-	rf_epa_gpio[5]	rf_epa_gpio[5]
					29	-	ant_switch_cntl[4]	ant_switch_cntl[4]
					30	Signal Name slave	epta_bl_act	epta_bl_act
						Signal Name master	epta_bl_act	epta_bl_act
					31	-	chip_clk_out[1]	-

表 3.1: 管脚定义 (continued)

QFN56	QFN68	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
27	35		DI/DO	PAD_GPIO_38	0	-	Data0	SD Host Data 0
					1	-	SPI1_MISO	SPI1 Master Input, Slave Output
					2	-	SFlash_D3	NOR FALSH controller signal2 Data 3
					3	-	I2S_DI/I2S_RCLK_O	I2S Data Input/I2S Receive Clock Output
					4	-	CANFD1_RX	CANFD1_RX
					5	-	I2C1_SDA	I2C 1 Serial Data
					6	-	I2C2_SCL	I2C 2 Serial Clock
					7	-	UART_SIG2	-
					8	-	-	-
					9	-	-	-
					10	-	-	-
					11	ir_rx_gpio_sel=0	SWGPIO[38]	Software GPIO 38
						ir_rx_gpio_sel=1	-	-
					12	-	SDIO_DAT0	SDIO_DAT0
					16	reg_pwm1_io_sel=0	pwm2_mc_out_c2p	PWM2 Channel 2 Positive
						reg_pwm1_io_sel=1	pwm1_mc_out_c3p	PWM1 Channel 3 Positive
					17	Signal Name	wl_jtag_tdo	WL JTAG Test Data Out
						Signal Name	-	-
					18	-	UART3_TXD	UART 3 Transmit Data
					19	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					20	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
					21	-	-	-
					22	-	-	-
					23	-	-	-
					24	Signal Name	-	-
						Signal Name	-	-
					25	-	spdt_p	spdt_p
					26	-	main_jtag_tdo	MAIN_JTAG_TDO
					27	-	PEC_38	PEC_38
					28	-	rf_epa_gpio[6]	rf_epa_gpio[6]
					29	-	ant_switch_cntl[5]	ant_switch_cntl[5]
					30	Signal Name slave	epta_bt_pri	epta_bt_pri
						Signal Name master	epta_bt_pri	epta_bt_pri
					31	-	chip_clk_out[2]	-

表 3.1: 管脚定义 (continued)

QFN56	QFN68	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
28	36		DI/DO	PAD_GPIO_39	0	-	Data1	SD Host Data 1
					1	-	SPI1_MOSI	SPI1 Master Output, Slave Input
					2	-	SFlash_CLK	NOR FALSH controller signal2 Clock
					3	-	I2S_DO/I2S_RCLK_O	I2S Data Output/I2S Receive Clock Output
					4	-	CANFD1_TX	CANFD1_TX
					5	-	I2C1_SCL	I2C 1 Serial Clock
					6	-	I2C2_SDA	I2C 2 Serial Data
					7	-	UART_SIG3	-
					8	-	-	-
					9	-	-	-
					10	-	-	-
					11	ir_rx_gpio_sel=0	SWGPIO[39]	Software GPIO 39
						ir_rx_gpio_sel=1	-	-
					12	-	SDIO_DAT1	SDIO_DAT1
					16	reg_pwm1_io_sel=0	pwm2_mc_out_c3p	PWM2 Channel 3 Positive
						reg_pwm1_io_sel=1	pwm1_mc_out_c3n	PWM1 Channel 3 Negative
					17	Signal Name	wl_jtag_tdi	WL JTAG Test Data Input
						Signal Name	-	-
					18	-	UART3_RXD	UART 3 Receive Data
					19	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					20	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
					21	-	-	-
					22	-	-	-
					23	-	-	-
					24	Signal Name	-	-
						Signal Name	-	-
					25	-	spdt_n	spdt_n
					26	-	main_jtag_tdi	MAIN_JTAG_TDI
					27	-	PEC_39	PEC_39
					28	-	rf_epa_gpio[7]	rf_epa_gpio[7]
					29	-	ant_switch_cntl[6]	ant_switch_cntl[6]
					30	Signal Name slave	-	-
						Signal Name master	-	-
					31	-	chip_clk_out[3]	-

表 3.1: 管脚定义 (continued)

QFN56	QFN68	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
29	37		DI/DO	PAD_GPIO_40	0	-	-	-
					1	-	SPI2_SS	SPI2 Slave Select
					2	-	pdm_0_in	PDM Data Line
					3	-	I2S_BCLK	I2S Bit Clock
					4	-	CANFD2_RX	CANFD2_RX
					5	-	I2C0_SDA	I2C 0 Serial Data
					6	-	I2C2_SCL	I2C 2 Serial Clock
					7	-	UART_SIG4	-
					8	-	-	-
					9	-	-	-
					10	-	USB_DP	-
					11	ir_rx_gpio_sel=0	SWGPIO[40]	Software GPIO 40
						ir_rx_gpio_sel=1	-	-
					12	-	-	-
					16	reg_pwm1_io_sel=0	pwm1_mc_out_c0p	PWM1 Channel 0 Positive
						reg_pwm1_io_sel=1	pwm2_mc_out_c0p	PWM2 Channel 0 Positive
					17	Signal Name	wl_jtag_tms/wl_cjtag_-tmsc	WL JTAG Test Mode Select/WL JTAG Test Mode Select and Control Counter
						Signal Name	ep_jtag_tms	EP JTAG Test Mode Select
					18	-	UART3_RTS	UART 3 Request To Send
					19	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					20	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
					21	-	-	-
					22	-	-	-
					23	-	-	-
					24	Signal Name	-	-
						Signal Name	-	-
					25	-	spdt_p	spdt_p
					26	-	main_jtag_tms/main_-cjtag_tmsc	MAIN_JTAG_TMS/MAIN JTAG Test Mode Select and Control Counter
					27	-	PEC_40	PEC_40
					28	-	rf_epa_gpio[0]	rf_epa_gpio[0]
					29	-	ant_switch_req	ant_switch_req
					30	Signal Name slave	epta_wl_act	epta_wl_act
						Signal Name master	epta_wl_act/gnt	epta_wl_act/gnt
					31	-	chip_clk_out[0]	-

表 3.1: 管脚定义 (continued)

QFN56	QFN68	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
30	38		DI/DO	PAD_GPIO_41	0	-	-	-
					1	-	SPI2_SCLK	SPI2 Serial Clock
					2	-	pdm_clk_o	PDM Clock Line
					3	-	I2S_FS	I2S Frame Sync
					4	-	CANFD2_TX	CANFD2_TX
					5	-	I2C0_SCL	I2C 0 Serial Clock
					6	-	I2C2_SDA	I2C 2 Serial Data
					7	-	UART_SIG5	-
					8	-	-	-
					9	-	-	-
					10	-	USB_DM	-
					11	ir_rx_gpio_sel=0	SWGPIO[41]	Software GPIO 41
						ir_rx_gpio_sel=1	-	-
					12	-	-	-
					16	reg_pwm1_io_sel=0	pwm1_mc_out_c1p	PWM1 Channel 1 Positive
						reg_pwm1_io_sel=1	pwm2_mc_out_c0n	PWM2 Channel 0 Negative
					17	Signal Name	wl_jtag_tclk/wl_cjtag_tckc	WL JTAG Test Clock
						Signal Name	ep_jtag_tclk	EP JTAG Test Clock
					18	-	UART3_CTS	UART 3 Clear To Send
					19	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					20	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
					21	-	-	-
					22	-	-	-
					23	-	-	-
					24	Signal Name	-	-
						Signal Name	-	-
					25	-	spdt_n	spdt_n
					26	-	main_jtag_tck/main_-cjtag_tckc	MAIN_JTAG_TCK
					27	-	PEC_41	PEC_41
					28	-	rf_epa_gpio[1]	rf_epa_gpio[1]
					29	-	ant_switch_cntl[0]	ant_switch_cntl[0]
					30	Signal Name slave	epta_bl_act	epta_bl_act
						Signal Name master	epta_bl_act	epta_bl_act
					31	-	chip_clk_out[1]	-

表 3.1: 管脚定义 (continued)

QFN56	QFN68	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
-	39		DI/DO	PAD_GPIO_42	0	-	-	-
					1	-	SPI2_MISO	SPI2 Master Input, Slave Output
					2	-	-	-
					3	-	I2S_DI/I2S_RCLK_O	I2S Data Input/I2S Receive Clock Output
					4	-	CANFD0_RX	CANFD0_RX
					5	-	I2C1_SDA	I2C 1 Serial Data
					6	-	I2C2_SCL	I2C 2 Serial Clock
					7	-	UART_SIG6	-
					8	-	-	-
					9	-	-	-
					10	-	vref_ext[3]	-
					11	ir_rx_gpio_sel=0	SWGPIO[42]	Software GPIO 42
						ir_rx_gpio_sel=1	-	-
					12	-	-	-
					16	reg_pwm1_io_sel=0	pwm1_mc_out_c2p	PWM1 Channel 2 Positive
						reg_pwm1_io_sel=1	pwm2_mc_out_c1p	PWM2 Channel 1 Positive
					17	Signal Name	wl_jtag_tdo	WL JTAG Test Data Out
						Signal Name	-	-
					18	-	UART3_TXD	UART 3 Transmit Data
					19	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					20	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
					21	-	-	-
					22	-	-	-
					23	-	-	-
					24	Signal Name	-	-
						Signal Name	-	-
					25	-	spdt_p	spdt_p
					26	-	main_jtag_tdo	MAIN_JTAG_TDO
					27	-	PEC_42	PEC_42
					28	-	rf_epa_gpio[2]	rf_epa_gpio[2]
					29	-	ant_switch_cntl[1]	ant_switch_cntl[1]
					30	Signal Name slave	epta_bt_pri	epta_bt_pri
						Signal Name master	epta_bt_pri	epta_bt_pri
					31	-	chip_clk_out[2]	-

表 3.1: 管脚定义 (continued)

QFN56	QFN68	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
31	40		DI/DO	PAD_GPIO_43	0	-	Data2	SD Host Data 2
					1	-	SPI2_MOSI	SPI2 Master Output, Slave Input
					2	-	SFlash_CS	NOR FALSH controller signal3 Chip Select
					3	-	I2S_DO/I2S_RCLK_O	I2S Data Output/I2S Receive Clock Output
					4	-	CANFD0_TX	CANFD0_TX
					5	-	I2C1_SCL	I2C 1 Serial Clock
					6	-	I2C2_SDA	I2C 2 Serial Data
					7	-	UART_SIG7	-
					8	-	-	-
					9	-	-	-
					10	-	-	-
					11	ir_rx_gpio_sel=0	SWGPIO[43]	Software GPIO 43
						ir_rx_gpio_sel=1	-	-
					12	-	SDIO_DAT2	SDIO_DAT2
					16	reg_pwm1_io_sel=0	pwm1_mc_out_c3p	PWM1 Channel 3 Positive
						reg_pwm1_io_sel=1	pwm2_mc_out_c1n	PWM2 Channel 1 Negative
					17	Signal Name	wl_jtag_tdi	WL JTAG Test Data Input
						Signal Name	-	-
					18	-	UART3_RXD	UART 3 Receive Data
					19	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					20	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
					21	-	-	-
					22	-	-	-
					23	-	-	-
					24	Signal Name	data22	-
						Signal Name	R6	-
					25	-	spdt_n	spdt_n
					26	-	main_jtag_tdi	MAIN_JTAG_TDI
					27	-	PEC_43	PEC_43
					28	-	rf_epa_gpio[3]	rf_epa_gpio[3]
					29	-	ant_switch_cntl[2]	ant_switch_cntl[2]
					30	Signal Name slave	-	-
						Signal Name master	-	-
					31	-	chip_clk_out[3]	-

表 3.1: 管脚定义 (continued)

QFN56	QFN68	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
32	41		DI/DO	PAD_GPIO_44	0	-	Data3	SD Host Data 3
					1	-	SPI3_SS	SPI3 Slave Select
					2	-	SFlash_D0	NOR FALSH controller signal3 Data 0
					3	-	I2S_BCLK	I2S Bit Clock
					4	-	CANFD1_RX	CANFD1_RX
					5	-	I2C0_SDA	I2C 0 Serial Data
					6	-	I2C2_SCL	I2C 2 Serial Clock
					7	-	UART_SIG8	-
					8	-	-	-
					9	-	-	-
					10	-	-	-
					11	ir_rx_gpio_sel=0	SWGPIO[44]	Software GPIO 44
						ir_rx_gpio_sel=1	-	-
					12	-	SDIO_DAT3	SDIO_DAT3
					16	reg_pwm1_io_sel=0	pwm2_mc_out_c0p	PWM2 Channel 0 Positive
						reg_pwm1_io_sel=1	pwm2_mc_out_c2p	PWM2 Channel 2 Positive
					17	Signal Name	wl_jtag_tms/wl_cjtag_-tmsc	WL JTAG Test Mode Select/WL JTAG Test Mode Select and Control Counter
						Signal Name	ep_jtag_tms	EP JTAG Test Mode Select
					18	-	UART3_RTS	UART 3 Request To Send
					19	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					20	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
					21	-	-	-
					22	-	-	-
					23	-	-	-
					24	Signal Name	data23	-
						Signal Name	R7	-
					25	-	spdt_p	spdt_p
					26	-	main_jtag_tms/main_-cjtag_tmsc	MAIN_JTAG_TMS/MAIN JTAG Test Mode Select and Control Counter
					27	-	PEC_44	PEC_44
					28	-	rf_epa_gpio[4]	rf_epa_gpio[4]
					29	-	ant_switch_cntl[3]	ant_switch_cntl[3]
					30	Signal Name slave	epta_wl_act	epta_wl_act
						Signal Name master	epta_wl_act/gnt	epta_wl_act/gnt
					31	-	chip_clk_out[0]	-

表 3.1: 管脚定义 (continued)

QFN56	QFN68	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
33	42		DI/DO	PAD_GPIO_45	0	-	CMD	SD Host Command
					1	-	SPI3_SCLK	SPI3 Serial Clock
					2	-	SFlash_D1	NOR FALSH controller signal3 Data 1
					3	-	I2S_FS	I2S Frame Sync
					4	-	CANFD1_TX	CANFD1_TX
					5	-	I2C0_SCL	I2C 0 Serial Clock
					6	-	I2C2_SDA	I2C 2 Serial Data
					7	-	UART_SIG9	-
					8	-	-	-
					9	-	-	-
					10	-	-	-
					11	ir_rx_gpio_sel=0	SWGPIO[45]	Software GPIO 45
						ir_rx_gpio_sel=1	-	-
					12	-	SDIO_CMD	SDIO_CMD
					16	reg_pwm1_io_sel=0	pwm2_mc_out_c1p	PWM2 Channel 1 Positive
						reg_pwm1_io_sel=1	pwm2_mc_out_c2n	PWM2 Channel 2 Negative
					17	Signal Name	wl_jtag_tclk/wl_cjtag_tckc	WL JTAG Test Clock
						Signal Name	ep_jtag_tclk	EP JTAG Test Clock
					18	-	UART30_CTS	UART 3 Clear To Send
					19	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					20	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
					21	-	-	-
					22	-	-	-
					23	-	-	-
					24	Signal Name	PCLK	-
						Signal Name	PCLK	-
					25	-	spdt_n	spdt_n
					26	-	main_jtag_tck/main_-cjtag_tckc	MAIN_JTAG_TCK
					27	-	PEC_45	PEC_45
					28	-	rf_epa_gpio[5]	rf_epa_gpio[5]
					29	-	ant_switch_cntl[4]	ant_switch_cntl[4]
					30	Signal Name slave	epta_bl_act	epta_bl_act
						Signal Name master	epta_bl_act	epta_bl_act
					31	-	chip_clk_out[1]	-
34	43			VDD_SDIO	-	-	-	-

表 3.1: 管脚定义 (continued)

QFN56	QFN68	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
35	44		DI/DO	PAD_GPIO_46	0	-	CLK	SD Host Clock
					1	-	SPI3_MISO	SPI3 Master Input, Slave Output
					2	-	SFlash_D2	NOR FALSH controller signal3 Data 2
					3	-	I2S_DI/I2S_RCLK_O	I2S Data Input/I2S Receive Clock Output
					4	-	CANFD2_RX	CANFD2_RX
					5	-	I2C1_SDA	I2C 1 Serial Data
					6	-	I2C2_SCL	I2C 2 Serial Clock
					7	-	UART_SIG10	-
					8	-	-	-
					9	-	-	-
					10	-	-	-
					11	ir_rx_gpio_sel=0	SWGPIO[46]	Software GPIO 46
						ir_rx_gpio_sel=1	-	-
					12	-	SDIO_CLK	SDIO_CLK
					16	reg_pwm1_io_sel=0	pwm2_mc_out_c2p	PWM2 Channel 2 Positive
						reg_pwm1_io_sel=1	pwm2_mc_out_c3p	PWM2 Channel 3 Positive
					17	Signal Name	wl_jtag_tdo	WL JTAG Test Data Out
						Signal Name	-	-
					18	-	UART3_TXD	UART 3 Transmit Data
					19	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					20	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
					21	-	-	-
					22	-	-	-
					23	-	-	-
					24	Signal Name	HS	-
						Signal Name	HS	-
					25	-	spdt_p	spdt_p
					26	-	main_jtag_tdo	MAIN_JTAG_TDO
					27	-	PEC_46	PEC_46
					28	-	rf_epa_gpio[6]	rf_epa_gpio[6]
					29	-	ant_switch_cntl[5]	ant_switch_cntl[5]
					30	Signal Name slave	epta_bt_pri	epta_bt_pri
						Signal Name master	epta_bt_pri	epta_bt_pri
					31	-	chip_clk_out[2]	-

表 3.1: 管脚定义 (continued)

QFN56	QFN68	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
36	45		DI/DO	PAD_GPIO_47	0	-	Data0	SD Host Data 0
					1	-	SPI3_MOSI	SPI3 Master Output, Slave Input
					2	-	SFlash_D3	NOR FALSH controller signal3 Data 3
					3	-	I2S_DO/I2S_RCLK_O	I2S Data Output/I2S Receive Clock Output
					4	-	CANFD2_TX	CANFD2_TX
					5	-	I2C1_SCL	I2C 1 Serial Clock
					6	-	I2C2_SDA	I2C 2 Serial Data
					7	-	UART_SIG11	-
					8	-	-	-
					9	-	-	-
					10	-	-	-
					11	ir_rx_gpio_sel=0	SWGPIO[47]	Software GPIO 47
						ir_rx_gpio_sel=1	-	-
					12	-	SDIO_DAT0	SDIO_DAT0
					16	reg_pwm1_io_sel=0	pwm2_mc_out_c3p	PWM2 Channel 3 Positive
						reg_pwm1_io_sel=1	pwm2_mc_out_c3n	PWM2 Channel 3 Negative
					17	Signal Name	wl_jtag_tdi	WL JTAG Test Data Input
						Signal Name	-	-
					18	-	UART3_RXD	UART 3 Receive Data
					19	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					20	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
					21	-	-	-
					22	-	-	-
					23	-	-	-
					24	Signal Name	VS	-
						Signal Name	VS	-
					25	-	spdt_n	spdt_n
					26	-	main_jtag_tdi	MAIN_JTAG_TDI
					27	-	PEC_47	PEC_47
					28	-	rf_epa_gpio[7]	rf_epa_gpio[7]
					29	-	ant_switch_cntl[6]	ant_switch_cntl[6]
					30	Signal Name slave	-	-
						Signal Name master	-	-
					31	-	chip_clk_out[3]	-

表 3.1: 管脚定义 (continued)

QFN56	QFN68	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
37	46		DI/DO	PAD_GPIO_48	0	-	Data1	SD Host Data 1
					1	-	SPI0_SS	SPI0 Slave Select
					2	-	SFlash_CLK	NOR FALSH controller signal3 Clock
					3	-	I2S_BCLK	I2S Bit Clock
					4	-	CANFD0_RX	CANFD0_RX
					5	-	I2C0_SDA	I2C 0 Serial Data
					6	-	I2C2_SCL	I2C 2 Serial Clock
					7	-	UART_SIG0	-
					8	-	-	-
					9	-	-	-
					10	-	-	-
					11	ir_rx_gpio_sel=0	SWGPIO[48]	Software GPIO 48
						ir_rx_gpio_sel=1	-	-
					12	-	SDIO_DAT1	SDIO_DAT1
					16	reg_pwm1_io_sel=0	pwm1_mc_out_c0p	PWM1 Channel 0 Positive
						reg_pwm1_io_sel=1	pwm1_mc_out_c2p	PWM1 Channel 2 Positive
					17	Signal Name	wl_jtag_tms/wl_cjtag_-tmsc	WL JTAG Test Mode Select/WL JTAG Test Mode Select and Control Counter
						Signal Name	ep_jtag_tms	EP JTAG Test Mode Select
					18	-	UART3_RTS	UART 3 Request To Send
					19	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					20	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
					21	-	-	-
					22	-	-	-
					23	-	-	-
					24	Signal Name	DE	-
						Signal Name	DE	-
					25	-	spdt_p	spdt_p
					26	-	main_jtag_tms/main_-cjtag_tmsc	MAIN_JTAG_TMS/MAIN JTAG Test Mode Select and Control Counter
					27	-	PEC_48	PEC_48
					28	-	rf_epa_gpio[0]	rf_epa_gpio[0]
					29	-	ant_switch_req	ant_switch_req
					30	Signal Name slave	-	-
						Signal Name master	-	-
					31	-	chip_clk_out[0]	-
38	47		Power,inout	VDDCORE	-	-	-	-
39	48		Power,Input	DCDC_OUT	-	-	-	-
40	49		Power,inout	VDD18	-	-	-	-
41	50		Analog	PU_CHIP	-	-	-	-
42	51		Power,Input	AVDD33	-	-	-	-
43	52		Clock	SW_DCDC	-	-	-	-

表 3.1: 管脚定义 (continued)

QFN56	QFN68	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
44	53		DI/DO	PAD_GPIO_0	0	-	-	-
					1	-	SPI0_SS	SPI0 Slave Select
					2	-	pdm_clk_o	PDM Clock Line
					3	-	I2S_BCLK	I2S Bit Clock
					4	-	CANFD0_RX	CANFD0_RX
					5	-	I2C0_SDA	I2C 0 Serial Data
					6	-	I2C2_SCL	I2C 2 Serial Clock
					7	-	UART_SIG0	-
					8	-	E1_REF_CLK	RMII Reference Clock
					9	-	CAM0_DATA0	Camera Data 0
					10	-	ADC0_6	-
					11	ir_rx_gpio_sel=0	SWGPIO[0]	Software GPIO 0
						ir_rx_gpio_sel=1	-	-
					12	-	irtx	irtx
					16	reg_pwm1_io_sel=0	pwm1_mc_out_c0p	PWM1 Channel 0 Positive
						reg_pwm1_io_sel=1	pwm1_mc_out_c0p	PWM1 Channel 0 Positive
					17	Signal Name	wl_jtag_tms/wl_cjtag_-tmsc	WL JTAG Test Mode Select/WL JTAG Test Mode Select and Control Counter
						Signal Name	ep_jtag_tms	EP JTAG Test Mode Select
					18	-	UART3_RTS	UART 3 Request To Send
					19	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					20	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
					21	-	AUDAC_PWM_P	AUDAC_PWM_P
					22	-	DBI_TypeB_DB0	Display Bus Interface Type B Data Bit 0
					23	-	DISP_QSPI_SCL	Display Quad SPI Serial Clock
					24	Signal Name	PCLK	-
						Signal Name	-	-
					25	-	spdt_p	spdt_p
					26	-	main_jtag_tms/main_-cjtag_tmsc	MAIN_JTAG_TMS/MAIN JTAG Test Mode Select and Control Counter
					27	-	PEC_0	PEC_0
					28	-	rf_epa_gpio[0]	rf_epa_gpio[0]
					29	-	ant_switch_req	ant_switch_req
					30	Signal Name slave	epta_wl_act/gnt	epta_wl_act/gnt
						Signal Name master	epta_wl_act/gnt	epta_wl_act/gnt
					31	-	chip_clk_out[0]	-

表 3.1: 管脚定义 (continued)

QFN56	QFN68	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
45	54		DI/DO	PAD_GPIO_1	0	-	-	-
					1	-	SPI0_SCLK	SPI0 Serial Clock
					2	-	pdm_0_in	PDM Data Line
					3	-	I2S_FS	I2S Frame Sync
					4	-	CANFD0_TX	CANFD0_TX
					5	-	I2C0_SCL	I2C 0 Serial Clock
					6	-	I2C2_SDA	I2C 2 Serial Data
					7	-	UART_SIG1	-
					8	-	E1_TXD[0]	RMII Transmit Data[0]
					9	-	CAM0_DATA1	Camera Data 1
					10	-	ADC1_6	-
					11	ir_rx_gpio_sel=0	SWGPIO[1]	Software GPIO 1
						ir_rx_gpio_sel=1	irrx	irrx
					12	-	irtx	irtx
					16	reg_pwm1_io_sel=0	pwm1_mc_out_c1p	PWM1 Channel 1 Positive
						reg_pwm1_io_sel=1	pwm1_mc_out_c0n	PWM1 Channel 0 Negative
					17	Signal Name	wl_jtag_tclk/wl_cjtag_tckc	WL JTAG Test Clock
						Signal Name	ep_jtag_tclk	EP JTAG Test Clock
					18	-	UART3_CTS	UART 3 Clear To Send
					19	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					20	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
					21	-	AUDAC_PWM_N	AUDAC_PWM_N
					22	-	DBI_TypeB_DB1	Display Bus Interface Type B Data Bit 1
					23	-	DISP_QSPI_CSn	Display Quad SPI Chip Select
					24	Signal Name	HS	-
						Signal Name	-	-
					25	-	spdt_n	spdt_n
					26	-	main_jtag_tck/main_-cjtag_tckc	MAIN_JTAG_TCK
					27	-	PEC_1	PEC_1
					28	-	rf_epa_gpio[1]	rf_epa_gpio[1]
					29	-	ant_switch_cntl[0]	ant_switch_cntl[0]
					30	Signal Name slave	epta_bl_act	epta_bl_act
						Signal Name master	epta_bl_act	epta_bl_act
					31	-	chip_clk_out[1]	-

表 3.1: 管脚定义 (continued)

QFN56	QFN68	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
46	55		DI/DO	PAD_GPIO_2	0	-	-	-
					1	-	SPI0_MISO	SPI0 Master Input, Slave Output
					2	-	pdm_clk_o	PDM Clock Line
					3	-	I2S_DI/I2S_RCLK_O	I2S Data Input/I2S Receive Clock Output
					4	-	CANFD1_RX	CANFD1_RX
					5	-	I2C1_SDA	I2C 1 Serial Data
					6	-	I2C2_SCL	I2C 2 Serial Clock
					7	-	UART_SIG2	-
					8	-	E1_TXD[1]	RMII Transmit Data[1]
					9	-	CAM0_DATA2	Camera Data 2
					10	-	ADC0_7	-
					11	ir_rx_gpio_sel=0	SWGPIO[2]	Software GPIO 2
						ir_rx_gpio_sel=1	irrx	irrx
					12	-	irtx	irtx
					16	reg_pwm1_io_sel=0	pwm1_mc_out_c2p	PWM1 Channel 2 Positive
						reg_pwm1_io_sel=1	pwm1_mc_out_c1p	PWM1 Channel 1 Positive
					17	Signal Name	wl_jtag_tdo	WL JTAG Test Data Out
						Signal Name	-	-
					18	-	UART3_TXD	UART 3 Transmit Data
					19	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					20	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
					21	-	AUDAC_PWM_P	AUDAC_PWM_P
					22	-	DBI_TypeB_DB2	Display Bus Interface Type B Data Bit 2
					23	-	DISP_QSPI_SDA0	Display Quad SPI Serial Data 0
					24	Signal Name	VS	-
						Signal Name	-	-
					25	-	spdt_p	spdt_p
					26	-	main_jtag_tdo	MAIN_JTAG_TDO
					27	-	PEC_2	PEC_2
					28	-	rf_epa_gpio[2]	rf_epa_gpio[2]
					29	-	ant_switch_cntl[1]	ant_switch_cntl[1]
					30	Signal Name slave	epta_bt_pri	epta_bt_pri
						Signal Name master	epta_bt_pri	epta_bt_pri
					31	-	chip_clk_out[2]	-

表 3.1: 管脚定义 (continued)

QFN56	QFN68	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
47	56		DI/DO	PAD_GPIO_3	0	-	-	-
					1	-	SPI0_MOSI	SPI0 Master Output, Slave Input
					2	-	pdm_0_in	PDM Data Line
					3	-	I2S_DO/I2S_RCLK_O	I2S Data Output/I2S Receive Clock Output
					4	-	CANFD1_TX	CANFD1_TX
					5	-	I2C1_SCL	I2C 1 Serial Clock
					6	-	I2C2_SDA	I2C 2 Serial Data
					7	-	UART_SIG3	-
					8	-	E1_RXD[0]	RMII Receive Data[0]
					9	-	CAM0_DATA3	Camera Data 3
					10	-	vref_ext[0]	-
					11	ir_rx_gpio_sel=0	SWGPIO[3]	Software GPIO 3
						ir_rx_gpio_sel=1	irrx	irrx
					12	-	irtx	irtx
					16	reg_pwm1_io_sel=0	pwm1_mc_out_c3p	PWM1 Channel 3 Positive
						reg_pwm1_io_sel=1	pwm1_mc_out_c1n	PWM1 Channel 1 Negative
					17	Signal Name	wl_jtag_tdi	WL JTAG Test Data Input
						Signal Name	-	-
					18	-	UART3_RXD	UART 3 Receive Data
					19	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					20	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
					21	-	AUDAC_PWM_N	AUDAC_PWM_N
					22	-	DBI_TypeB_DB3	Display Bus Interface Type B Data Bit 3
					23	-	DISP_QSPI_SDA1	Display Quad SPI Serial Data 1
					24	Signal Name	DE	-
						Signal Name	-	-
					25	-	spdt_n	spdt_n
					26	-	main_jtag_tdi	MAIN_JTAG_TDI
					27	-	PEC_3	PEC_3
					28	-	rf_epa_gpio[3]	rf_epa_gpio[3]
					29	-	ant_switch_cntl[2]	ant_switch_cntl[2]
					30	Signal Name slave	-	-
						Signal Name master	-	-
					31	-	chip_clk_out[3]	-

表 3.1: 管脚定义 (continued)

QFN56	QFN68	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
48	57		DI/DO	PAD_GPIO_4	0	-	-	-
					1	-	SPI1_SS	SPI1 Slave Select
					2	-	pdm_clk_o	PDM Clock Line
					3	-	I2S_BCLK	I2S Bit Clock
					4	-	CANFD2_RX	CANFD2_RX
					5	-	I2C0_SDA	I2C 0 Serial Data
					6	-	I2C2_SCL	I2C 2 Serial Clock
					7	-	UART_SIG4	-
					8	-	E1_RXD[1]	RMII Receive Data[1]
					9	-	CAM0_HSYNC	Camera Horizontal Sync
					10	-	ADC1_7/AUADC_-6/xtal32k_in	-
					11	ir_rx_gpio_sel=0	SWGPIO[4]	Software GPIO 4
						ir_rx_gpio_sel=1	irrx	irrx
					12	-	irtx	irtx
					16	reg_pwm1_io_sel=0	pwm2_mc_out_c0p	PWM2 Channel 0 Positive
						reg_pwm1_io_sel=1	pwm1_mc_out_c2p	PWM1 Channel 2 Positive
					17	Signal Name	wl_jtag_tms/wl_cjtag_-tmsc	WL JTAG Test Mode Select/WL JTAG Test Mode Select and Control Counter
						Signal Name	ep_jtag_tms	EP JTAG Test Mode Select
					18	-	UART3_RTS	UART 3 Request To Send
					19	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					20	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
					21	-	-	-
					22	-	DBI_TypeB_DB4	Display Bus Interface Type B Data Bit 4
					23	-	DISP_QSPI_SDA2	Display Quad SPI Serial Data 2
					24	Signal Name	PCLK	-
						Signal Name	-	-
					25	-	spdt_p	spdt_p
					26	-	main_jtag_tms/main_-cjtag_tmsc	MAIN_JTAG_TMS/MAIN JTAG Test Mode Select and Control Counter
					27	-	PEC_4	PEC_4
					28	-	rf_epa_gpio[4]	rf_epa_gpio[4]
					29	-	ant_switch_cntl[3]	ant_switch_cntl[3]
					30	Signal Name slave	epta_wl_act	epta_wl_act
						Signal Name master	epta_wl_act/gnt	epta_wl_act/gnt
					31	-	chip_clk_out[0]	-

表 3.1: 管脚定义 (continued)

QFN56	QFN68	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
49	58		DI/DO	PAD_GPIO_5	0	-	-	-
					1	-	SPI1_SCLK	SPI1 Serial Clock
					2	-	pdm_0_in	PDM Data Line
					3	-	I2S_FS	I2S Frame Sync
					4	-	CANFD2_TX	CANFD2_TX
					5	-	I2C0_SCL	I2C 0 Serial Clock
					6	-	I2C2_SDA	I2C 2 Serial Data
					7	-	UART_SIG5	-
					8	-	E1_RX_ERR	-
					9	-	CAM0_VSYNC	Camera Vertical Sync
					10	-	ADC0_8/AUADC_7/xtal_ext_clk_18/xtal32k_out	-
					11	ir_rx_gpio_sel=0	SWGPIO[5]	Software GPIO 5
						ir_rx_gpio_sel=1	irrx	irrx
					12	-	irtx	irtx
					16	reg_pwm1_io_sel=0	pwm2_mc_out_c1p	PWM2 Channel 1 Positive
						reg_pwm1_io_sel=1	pwm1_mc_out_c2n	PWM1 Channel 2 Negative
					17	Signal Name	wl_jtag_tclk/wl_cjtag_tckc	WL JTAG Test Clock
						Signal Name	ep_jtag_tclk	EP JTAG Test Clock
					18	-	UART3_CTS	UART 3 Clear To Send
					19	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					20	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
					21	-	AUDAC_PWM_P	AUDAC_PWM_P
					22	-	DBI_TypeB_DB5	Display Bus Interface Type B Data Bit 5
					23	-	DISP_QSPI_SDA3	Display Quad SPI Serial Data 3
					24	Signal Name	HS	-
						Signal Name	-	-
					25	-	spdt_n	spdt_n
					26	-	main_jtag_tck/main_cjtag_tckc	MAIN_JTAG_TCK
					27	-	PEC_5	PEC_5
					28	-	rf_epa_gpio[5]	rf_epa_gpio[5]
					29	-	ant_switch_cntl[4]	ant_switch_cntl[4]
					30	Signal Name slave	epta_bl_act	epta_bl_act
						Signal Name master	epta_bl_act	epta_bl_act
					31	-	chip_clk_out[1]	-

表 3.1: 管脚定义 (continued)

QFN56	QFN68	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
50	59		DI/DO	PAD_GPIO_6	0	-	-	-
					1	-	SPI1_MISO	SPI1 Master Input, Slave Output
					2	-	pdm_clk_o	PDM Clock Line
					3	-	I2S_DI/I2S_RCLK_O	I2S Data Input/I2S Receive Clock Output
					4	-	CANFD0_RX	CANFD0_RX
					5	-	I2C1_SDA	I2C 1 Serial Data
					6	-	I2C2_SCL	I2C 2 Serial Clock
					7	-	UART_SIG6	-
					8	-	E1_TX_EN	RMII Transmit Enable
					9	-	CAM0_CLK	Camera Clock
					10	-	ADC1_8/touch_ch[0]	-
					11	ir_rx_gpio_sel=0	SWGPIO[6]	Software GPIO 6
						ir_rx_gpio_sel=1	irrx	irrx
					12	-	irtx	irtx
					16	reg_pwm1_io_sel=0	pwm2_mc_out_c2p	PWM2 Channel 2 Positive
						reg_pwm1_io_sel=1	pwm1_mc_out_c3p	PWM1 Channel 3 Positive
					17	Signal Name	wl_jtag_tdo	WL JTAG Test Data Out
						Signal Name	-	-
					18	-	UART3_TXD	UART 3 Transmit Data
					19	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					20	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
					21	-	AUDAC_PWM_N	AUDAC_PWM_N
					22	-	DBI_TypeB_DB6	Display Bus Interface Type B Data Bit 6
					23	-	-	-
					24	Signal Name	VS	-
						Signal Name	-	-
					25	-	spdt_p	spdt_p
					26	-	main_jtag_tdo	MAIN_JTAG_TDO
					27	-	PEC_6	PEC_6
					28	-	rf_epa_gpio[6]	rf_epa_gpio[6]
					29	-	ant_switch_cntl[5]	ant_switch_cntl[5]
					30	Signal Name slave	epta_bt_pri	epta_bt_pri
						Signal Name master	epta_bt_pri	epta_bt_pri
					31	-	chip_clk_out[2]	-

表 3.1: 管脚定义 (continued)

QFN56	QFN68	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
51	60		DI/DO	PAD_GPIO_7	0	-	-	-
					1	-	SPI1_MOSI	SPI1 Master Output, Slave Input
					2	-	pdm_0_in	PDM Data Line
					3	-	I2S_DO/I2S_RCLK_O	I2S Data Output/I2S Receive Clock Output
					4	-	CANFD0_TX	CANFD0_TX
					5	-	I2C1_SCL	I2C 1 Serial Clock
					6	-	I2C2_SDA	I2C 2 Serial Data
					7	-	UART_SIG7	-
					8	-	E1_RX_DV	RMII Receive Data Valid
					9	-	CAM0_DATA4	Camera Data 4
					10	-	ADC0_9/touch_ch[1]	-
					11	ir_rx_gpio_sel=0	SWGPIO[7]	Software GPIO 7
						ir_rx_gpio_sel=1	irrx	irrx
					12	-	irtx	irtx
					16	reg_pwm1_io_sel=0	pwm2_mc_out_c3p	PWM2 Channel 3 Positive
						reg_pwm1_io_sel=1	pwm1_mc_out_c3n	PWM1 Channel 3 Negative
					17	Signal Name	wl_jtag_tdi	WL JTAG Test Data Input
						Signal Name	-	-
					18	-	UART3_RXD	UART 3 Receive Data
					19	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					20	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
					21	-	AUDAC_PWM_P	AUDAC_PWM_P
					22	-	DBI_TypeB_DB7	Display Bus Interface Type B Data Bit 7
					23	-	-	-
					24	Signal Name	DE	-
						Signal Name	-	-
					25	-	spdt_n	spdt_n
					26	-	main_jtag_tdi	MAIN_JTAG_TDI
					27	-	PEC_7	PEC_7
					28	-	rf_epa_gpio[7]	rf_epa_gpio[7]
					29	-	ant_switch_cntl[6]	ant_switch_cntl[6]
					30	Signal Name slave	-	-
						Signal Name master	-	-
					31	-	chip_clk_out[3]	-

表 3.1: 管脚定义 (continued)

QFN56	QFN68	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
-	61		DI/DO	PAD_GPIO_8	0	-	-	-
					1	-	SPI2_SS	SPI2 Slave Select
					2	-	pdm_clk_o	PDM Clock Line
					3	-	I2S_BCLK	I2S Bit Clock
					4	-	CANFD1_RX	CANFD1_RX
					5	-	I2C0_SDA	I2C 0 Serial Data
					6	-	I2C2_SCL	I2C 2 Serial Clock
					7	-	UART_SIG8	-
					8	-	-	-
					9	-	CAM0_DATA5	Camera Data 5
					10	-	ADC1_9	-
					11	ir_rx_gpio_sel=0	SWGPIO[8]	Software GPIO 8
						ir_rx_gpio_sel=1	irrx	irrx
					12	-	-	-
					16	reg_pwm1_io_sel=0	pwm1_mc_out_c0p	PWM1 Channel 0 Positive
						reg_pwm1_io_sel=1	pwm2_mc_out_c0p	PWM2 Channel 0 Positive
					17	Signal Name	wl_jtag_tms/wl_cjtag_-tmsc	WL JTAG Test Mode Select/WL JTAG Test Mode Select and Control Counter
						Signal Name	ep_jtag_tms	EP JTAG Test Mode Select
					18	-	UART3_RTS	UART 3 Request To Send
					19	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					20	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
					21	-	AUDAC_PWM_N	AUDAC_PWM_N
					22	-	-	-
					23	-	-	-
					24	Signal Name	-	-
						Signal Name	-	-
					25	-	spdt_p	spdt_p
					26	-	main_jtag_tms/main_-cjtag_tmsc	MAIN_JTAG_TMS/MAIN JTAG Test Mode Select and Control Counter
					27	-	PEC_8	PEC_8
					28	-	rf_epa_gpio[0]	rf_epa_gpio[0]
					29	-	ant_switch_req	ant_switch_req
					30	Signal Name slave	epta_wl_act	epta_wl_act
						Signal Name master	epta_wl_act/gnt	epta_wl_act/gnt
					31	-	chip_clk_out[0]	-

表 3.1: 管脚定义 (continued)

QFN56	QFN68	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
-	62		DI/DO	PAD_GPIO_9	0	-	-	-
					1	-	SPI2_SCLK	SPI2 Serial Clock
					2	-	pdm_0_in	PDM Data Line
					3	-	I2S_FS	I2S Frame Sync
					4	-	CANFD1_TX	CANFD1_TX
					5	-	I2C0_SCL	I2C 0 Serial Clock
					6	-	I2C2_SDA	I2C 2 Serial Data
					7	-	UART_SIG9	-
					8	-	-	-
					9	-	CAM0_DATA6	Camera Data 6
					10	-	ADC0_10	-
					11	ir_rx_gpio_sel=0	SWGPIO[9]	Software GPIO 9
						ir_rx_gpio_sel=1	irrx	irrx
					12	-	-	-
					16	reg_pwm1_io_sel=0	pwm1_mc_out_c1p	PWM1 Channel 1 Positive
						reg_pwm1_io_sel=1	pwm2_mc_out_c0n	PWM2 Channel 0 Negative
					17	Signal Name	wl_jtag_tclk/wl_cjtag_tckc	WL JTAG Test Clock
						Signal Name	ep_jtag_tclk	EP JTAG Test Clock
					18	-	UART3_CTS	UART 3 Clear To Send
					19	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					20	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
					21	-	AUDAC_PWM_P	AUDAC_PWM_P
					22	-	-	-
					23	-	-	-
					24	Signal Name	-	-
						Signal Name	-	-
					25	-	spdt_n	spdt_n
					26	-	main_jtag_tck/main_-cjtag_tckc	MAIN_JTAG_TCK
					27	-	PEC_9	PEC_9
					28	-	rf_epa_gpio[1]	rf_epa_gpio[1]
					29	-	ant_switch_cntl[0]	ant_switch_cntl[0]
					30	Signal Name slave	epta_bl_act	epta_bl_act
						Signal Name master	epta_bl_act	epta_bl_act
					31	-	chip_clk_out[1]	-

表 3.1: 管脚定义 (continued)

QFN56	QFN68	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
-	63		DI/DO	PAD_GPIO_10	0	-	-	-
					1	-	SPI2_MISO	SPI2 Master Input, Slave Output
					2	-	pdm_clk_o	PDM Clock Line
					3	-	I2S_DI/I2S_RCLK_O	I2S Data Input/I2S Receive Clock Output
					4	-	CANFD2_RX	CANFD2_RX
					5	-	I2C1_SDA	I2C 1 Serial Data
					6	-	I2C2_SCL	I2C 2 Serial Clock
					7	-	UART_SIG10	-
					8	-	-	-
					9	-	CAM0_DATA7	Camera Data 7
					10	-	ADC1_10	-
					11	ir_rx_gpio_sel=0	SWGPIO[10]	Software GPIO 10
						ir_rx_gpio_sel=1	irrx	irrx
					12	-	-	-
					16	reg_pwm1_io_sel=0	pwm1_mc_out_c2p	PWM1 Channel 2 Positive
						reg_pwm1_io_sel=1	pwm2_mc_out_c1p	PWM2 Channel 1 Positive
					17	Signal Name	wl_jtag_tdo	WL JTAG Test Data Out
						Signal Name	-	-
					18	-	UART3_TXD	UART 3 Transmit Data
					19	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					20	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
					21	-	AUDAC_PWM_N	AUDAC_PWM_N
					22	-	-	-
					23	-	-	-
					24	Signal Name	-	-
						Signal Name	-	-
					25	-	spdt_p	spdt_p
					26	-	main_jtag_tdo	MAIN_JTAG_TDO
					27	-	PEC_10	PEC_10
					28	-	rf_epa_gpio[2]	rf_epa_gpio[2]
					29	-	ant_switch_cntl[1]	ant_switch_cntl[1]
					30	Signal Name slave	epta_bt_pri	epta_bt_pri
						Signal Name master	epta_bt_pri	epta_bt_pri
					31	-	chip_clk_out[2]	-
52	64		Clock	XTAL_OUT	-	-	-	-
53	65		Clock	XTAL_IN	-	-	-	-
54	66		Power,Input	AVDD_RF1	-	-	-	-
55	67		Power,Input	AVDD33_RF1	-	-	-	-
56	68		Power,Input	AVDD33_RF2	-	-	-	-

[1] UART SIGx(x=0-11) 用于选择 UART 信号的映射，以 UART_SIG0 和 UART_SIG1 为例，下表为 UART_SIG0 和 UART_SIG1 的映射关系。

[2] 当选为 SPI 功能时，默认为 SPI_MISO，可通过寄存器将该功能转换为 SPI_MOSI。

[3] SF1 用于内部 flash，SF2 和 SF3 不能同时使用。

表 3.2: UART Signal Mapping

UART Signal	uart_sig_0_sel	Mapping Signal
UART_SIG0	uart_sig_0_sel=0	UART0_RTS
	uart_sig_0_sel=1	UART0_CTS
	uart_sig_0_sel=2	UART0_TXD
	uart_sig_0_sel=3	UART0_RXD
	uart_sig_0_sel=4	UART1_RTS
	uart_sig_0_sel=5	UART1_CTS
	uart_sig_0_sel=6	UART1_TXD
	uart_sig_0_sel=7	UART1_RXD
	uart_sig_0_sel=8	UART2_RTS
	uart_sig_0_sel=9	UART2_CTS
	uart_sig_0_sel=10	UART2_TXD
	uart_sig_0_sel=11	UART2_RXD
UART_SIG1	uart_sig_1_sel=0	UART0_RTS
	uart_sig_1_sel=1	UART0_CTS
	uart_sig_1_sel=2	UART0_TXD
	uart_sig_1_sel=3	UART0_RXD
	uart_sig_1_sel=4	UART1_RTS
	uart_sig_1_sel=5	UART1_CTS
	uart_sig_1_sel=6	UART1_TXD
	uart_sig_1_sel=7	UART1_RXD
	uart_sig_1_sel=8	UART2_RTS
	uart_sig_1_sel=9	UART2_CTS
	uart_sig_1_sel=10	UART2_TXD
	uart_sig_1_sel=11	UART2_RXD

4 射频特性

射频接收和传输模式的特性，如下表所示：

表 4.1: WLAN RX 射频特性

模式		备注	Performance @3.3V,25℃			
			最小值	典型值	最大值	单位
接收灵敏度 2G	11ax - MCS0 HE20			TBD		dBm
	11ax - MCS9 HE20	LDPC		-70		
	11ax - MCS0 HE40			TBD		
	11ax - MCS9 HE40	LDPC		-67		
	11n - MCS0 HT20			TBD		
	11n - MCS7 HT20	LDPC		-76		
	11n - MCS0 HT40			TBD		
	11n - MCS7 HT40	LDPC		-73		
	11g - 6Mbps			TBD		
	11g - 54Mbps			-77		
	11b - 1Mbps			TBD		
	11b - 11Mbps			-90		
最大接收水平 2G	11ax - MCS0 HE20			TBD		dBm
	11ax - MCS9 HE20			>-10		
	11n - MCS0 HT20			TBD		
	11n - MCS7 HT20			>-10		
	11g - 6Mbps			TBD		
	11g - 54Mbps			TBD		
	11b - 1Mbps			TBD		
	11b - 11Mbps			>5		

表 4.1: WLAN RX 射频特性 (continued)

模式		备注	Performance @3.3V,25℃			
			最小值	典型值	最大值	单位
相邻信道抑制	11ax - MCS0 HE20	LDPC		TBD		dB
	11ax - MCS9 HE20	LDPC		TBD		
	11n - MCS0 HT20	LDPC		TBD		
	11n - MCS7 HT20	LDPC		TBD		
	11g - 6Mbps			TBD		
	11g - 54Mbps			TBD		
	11b - 1Mbps			TBD		
	11b - 11Mbps			TBD		
S11				<-10		dB
接收灵敏度 5G	11ax - MCS0 HE20			TBD		dBm
	11ax - MCS9 HE20	LDPC		-68		
	11ax - MCS0 HE40			TBD		
	11ax - MCS9 HE40	LDPC		-65		
	11ax - MCS11 HE80	LDPC		TBD		
	11n - MCS0 HT20			TBD		
	11n - MCS7 HT20	LDPC		-74		
	11n - MCS0 HT40			TBD		
	11n - MCS7 HT40	LDPC		-71		
	11g - 6Mbps			TBD		
	11g - 54Mbps			-75		
	11a - 1Mbps			TBD		
	11a - 11Mbps			TBD		
最大接收水平 5G	11ax - MCS0 HE20			TBD		dBm
	11ax - MCS9 HE20			>-10		
	11n - MCS0 HT20			TBD		
	11n - MCS7 HT20			>-10		
	11g - 6Mbps			TBD		
	11g - 54Mbps			TBD		
	11a - 1Mbps			TBD		
	11a - 11Mbps			TBD		

表 4.1: WLAN RX 射频特性 (continued)

模式		备注	Performance @3.3V,25°C			
			最小值	典型值	最大值	单位
相邻信道抑制	11ax - MCS0 HE20	LDPC		TBD		dB
	11ax - MCS9 HE20	LDPC		TBD		
	11n - MCS0 HT20	LDPC		TBD		
	11n - MCS7 HT20	LDPC		TBD		
	11g - 6Mbps			TBD		
	11g - 54Mbps			TBD		
	11b - 1Mbps			TBD		
	11b - 11Mbps			TBD		
S11				<-10		dB

表 4.2: WLAN TX 射频特性

模式		备注	Performance @3.3V,25°C			
			最小值	典型值	最大值	单位
发射功率 2G	11ax - MCS0 HE20			TBD		dBm
	11ax - MCS9 HE20	BCC		16		
	11ax - MCS0 HE40			TBD		
	11ax - MCS9 HE40			14		
	11ax - MCS11 HE40			TBD		
	11n - MCS0 HT20			TBD		
	11n - MCS7 HT20			17		
	11n - MCS0 HT40			TBD		
	11n - MCS7 HT40			16		
	11g - 6Mbps			TBD		
	11g - 54Mbps			18		
	11b - 1Mbps			TBD		
	11b - 11Mbps			21		

表 4.2: WLAN TX 射频特性 (continued)

模式		备注	Performance @3.3V,25°C			
			最小值	典型值	最大值	单位
发射功率 5G	11ax - MCS0 HE20			TBD		dBm
	11ax - MCS9 HE20	BCC		15		
	11ax - MCS0 HE40			TBD		
	11ax - MCS9 HE40			13		
	11ax - MCS0 HE80			TBD		
	11ax - MCS11 HE80			TBD		
	11n - MCS0 HT20			TBD		
	11n - MCS7 HT20			16		
	11n - MCS0 HT40			TBD		
	11n - MCS7 HT40			15		
	11g - 6Mbps			TBD		
	11g - 54Mbps			17		
	11a - 1Mbps			TBD		
	11a - 11Mbps			20		
误差矢量幅度	11ax - MCS9 HE20			TBD		dB
	11n - MCS7 HT20			TBD		
	11g - 54Mbps			TBD		
Accuracy of power control	1dB/step			TBD		

表 4.3: BLE RX 射频特性

模式		备注	Performance @3.3V,25°C			
			最小值	典型值	最大值	单位
接收机灵敏度	1Mbps	Packet Length 37bytes, Dirty Transmitter off		-97.5		dBm
		Packet Length 37bytes, Dirty Transmitter on		TBD		
	2Mbps	Packet Length 37bytes, Dirty Transmitter off		-95		
		Packet Length 37bytes, Dirty Transmitter on		TBD		
	S2 (500Kbps)	Packet Length 37bytes, Dirty Transmitter off		TBD		

表 4.3: BLE RX 射频特性 (continued)

模式		备注	Performance @3.3V,25°C			
			最小值	典型值	最大值	单位
		Packet Length 37bytes, Dirty Transmitter on		TBD		
	S8 (125Kbps)	Packet Length 37bytes, Dirty Transmitter off		TBD		
		Packet Length 37bytes, Dirty Transmitter on		TBD		
最大接收电平	1Mbps			>5		
	2Mbps			>5		
干扰抑制性能	1Mbps, F = F_0			TBD		dB
	1Mbps, F = F_0+ 1MHz			TBD		
	1Mbps, F = F_0- 1MHz			TBD		
	1Mbps, F = F_0+ 2MHz			TBD		
	1Mbps, F = F_0- 2MHz			TBD		
	1Mbps, F = F_0+ 3MHz			TBD		
	1Mbps, F = F_0- 3MHz			TBD		
	2Mbps, F = F_0			TBD		
	2Mbps, F = F_0+ 2MHz			TBD		
	2Mbps, F = F_0- 2MHz			TBD		
	2Mbps, F = F_0+ 4MHz			TBD		
	2Mbps, F = F_0- 4MHz			TBD		
	2Mbps, F = F_0+ 6MHz			TBD		
	2Mbps, F = F_0- 6MHz			TBD		
	S2 (500Kbps), F = F_0			TBD		
	S2 (500Kbps), F = F_0+ 1MHz			TBD		
	S2 (500Kbps), F = F_0- 1MHz			TBD		
	S2 (500Kbps), F = F_0+ 2MHz			TBD		
	S2 (500Kbps), F = F_0- 2MHz			TBD		
	S2 (500Kbps), F = F_0+ 3MHz			TBD		
	S2 (500Kbps), F = F_0- 3MHz			TBD		

表 4.3: BLE RX 射频特性 (continued)

模式		备注	Performance @3.3V,25°C			
			最小值	典型值	最大值	单位
	S8 (125Kbps), F = F_0			TBD		
	S8 (125Kbps), F = F_0+ 1MHz			TBD		
	S8 (125Kbps), F = F_0- 1MHz			TBD		
	S8 (125Kbps), F = F_0+ 2MHz			TBD		
	S8 (125Kbps), F = F_0- 2MHz			TBD		
	S8 (125Kbps), F = F_0+ 3MHz			TBD		
	S8 (125Kbps), F = F_0- 3MHz			TBD		

表 4.4: BLE TX 射频特性

模式		备注	Performance @3.3V,25°C			
			最小值	典型值	最大值	单位
调制特性	1Mbps, Δf1avg			TBD		KHz
	1Mbps, Δf2max > 185KHz			TBD		%
	1Mbps, Δf2avg/Δf1avg			TBD		
	2Mbps, Δf1avg			TBD		KHz
	2Mbps, Δf2max > 370KHz			TBD		%
	2Mbps, Δf2avg/Δf1avg			TBD		
	S8 (125Kbps), Δf1avg			TBD		KHz
	S8 (125Kbps), Δf1max > 185KHz			TBD		%

表 4.4: BLE TX 射频特性 (continued)

模式		备注	Performance @3.3V,25°C			
			最小值	典型值	最大值	单位
载波特性	1Mbps, $\|f_n\|$			TBD		KHz
	1Mbps, $\|f_0 - f_n\|$			TBD		
	1Mbps, $\|f_1 - f_0\|$			TBD		
	1Mbps, $\|f_n - f_{(n-5)}\|$			TBD		
	2Mbps, $\|f_n\|$			TBD		
	2Mbps, $\|f_0 - f_n\|$			TBD		
	2Mbps, $\|f_1 - f_0\|$			TBD		
	2Mbps, $\|f_n - f_{(n-5)}\|$			TBD		
	S8 (125Kbps), $\|f_n\|$			TBD		
	S8 (125Kbps), $\|f_0 - f_n\|$			TBD		
	S8 (125Kbps), $\|f_0 - f_3\|$			TBD		
	S8 (125Kbps), $\|f_n - f_{(n-3)}\|$			TBD		
带内杂散	1Mbps, F = $F_0 \pm$ 2MHz			TBD		dBm
	1Mbps, F = $F_0 \pm$ 3MHz			TBD		
	2Mbps, F = $F_0 \pm$ 4MHz			TBD		
	2Mbps, F = $F_0 \pm$ 5MHz			TBD		
	2Mbps, F = $F_0 \pm$ 6MHz			TBD		
发射功率	1Mbps			10		dBm

表 4.5: BT RX 射频特性

模式		备注	Performance @3.3V,25°C			
			最小值	典型值	最大值	单位
接收机灵敏度	BR 1Mbps Multi-slot	0.1% BER, Dirty Transmitter off		-93		dBm
		0.1% BER, Dirty Transmitter on		TBD		
	EDR 2Mbps Multi-slot	0.01% BER, Dirty Transmitter off		-95		
		0.01% BER, Dirty Transmitter on		TBD		
	EDR 3Mbps Multi-slot	0.01% BER, Dirty Transmitter off		TBD		
		0.01% BER, Dirty Transmitter on		TBD		

表 4.5: BT RX 射频特性 (continued)

模式		备注	Performance @3.3V,25°C			
			最小值	典型值	最大值	单位
最大接收电平	BR 1Mbps Single-slot	0.1% BER		TBD		
	EDR 2Mbps Multi-slot	0.1% BER		TBD		
	EDR 3Mbps Multi-slot	0.1% BER		TBD		

表 4.6: BT TX 射频特性

模式		备注	Performance @3.3V,25°C			
			最小值	典型值	最大值	单位
调制特性	BR 1Mbps, Δf1avg			TBD		KHz
	BR 1Mbps, Δf2max > 115KHz			TBD		%
	BR 1Mbps, Δf2avg/Δf1avg			TBD		
	EDR 2Mbps, RMS DEVM			TBD		%
	EDR 2Mbps, Peak DEVM			TBD		
	EDR 2Mbps, 99% DEVM			TBD		
	EDR 3Mbps, RMS DEVM			TBD		
	EDR 3Mbps, Peak DEVM			TBD		
	EDR 3Mbps, 99% DEVM			TBD		
载波特性	BR 1Mbps, $\lvert f_0 \rvert$			TBD		KHz
	BR 1Mbps, $\lvert f_0 - f_k \rvert$			TBD		
	BR 1Mbps, $\lvert f_{(k+5)} - f_k \rvert$			TBD		
	EDR 2Mbps, $\lvert \omega_i \rvert$			TBD		
	EDR 2Mbps, $\lvert \omega_i + \omega_0 \rvert$			TBD		
	EDR 2Mbps, $\lvert \omega_0 \rvert$			TBD		
	EDR 3Mbps, $\lvert \omega_i \rvert$			TBD		
	EDR 3Mbps, $\lvert \omega_i + \omega_0 \rvert$			TBD		
	EDR 3Mbps, $\lvert \omega_0 \rvert$			TBD		
邻信道辐射功率	BR 1Mbps, F = $F_0 \pm$ 2MHz			TBD		dBm
	BR 1Mbps, F = $F_0 \pm$ 3MHz			TBD		

表 4.6: BT TX 射频特性 (continued)

模式		备注	Performance @3.3V,25°C			
			最小值	典型值	最大值	单位
带内杂散	EDR 2Mbps, F = F_0± 1MHz	PTX-26dB		TBD		
	EDR 2Mbps, F = F_0± 2MHz			TBD		
	EDR 2Mbps, F = F_0± 3MHz			TBD		
	EDR 3Mbps, F = F_0± 1MHz	PTX-26dB		TBD		
	EDR 3Mbps, F = F_0± 2MHz			TBD		
	EDR 3Mbps, F = F_0± 3MHz			TBD		
发射功率	BR			10		dBm
	EDR			8		

表 4.7: ZigBee RX 射频特性

模式		备注	Performance @3.3V,25°C			
			最小值	典型值	最大值	单位
接收灵敏度	250Kbps			-104		dBm
最大接收电平	250Kbps			>5		

表 4.8: ZigBee TX 射频特性

模式		备注	Performance @3.3V,25°C			
			最小值	典型值	最大值	单位
发射功率	250Kbps			10		dBm
误差矢量幅度	250Kbps			TBD		%

5 功耗

TBD

6 电气特性

6.1 绝对最大额定值

表 6.1: 电源的绝对最大额定值

管脚名称	最小值	最大值	单位
AVDD33_RF1, AVDD33_RF2, AVDD33_RF3, AVDD33	-0.3	3.63	V
VDDIO	-0.3	3.63	V
VDD_SDIO	-0.3	3.63	V
ESD Protection (HBM)		2000	V
Storage Temperature	-45	135	°C

6.2 运行条件

6.2.1 电源特性

表 6.2: 建议电源值范围

管脚名称	最小值	典型值	最大值	单位
AVDD33_RF1, AVDD33_RF2, AVDD33_RF3, AVDD33	2.97	3.3	3.63	V
VDDIO	2.97	3.3	3.63	
VDD_SDIO	2.97/1.62	3.3/1.8	3.63/1.98	

6.2.2 IO 直流特性

测试条件：IO 供电 VDDIO = 3.3V，温度 25°C

表 6.3: IO 直流特性

符号	描述	条件	最小值	典型值	最大值	单位
VOH	Output voltage high	GPIO drive strength 0, source current = 7.62mA		0.9*VDDIO		V
		GPIO drive strength 1, source current = 15.21mA				
		GPIO drive strength 2, source current = 22.74mA				
		GPIO drive strength 3, source current = 30.27mA				
VOL	Output voltage low	GPIO drive strength 0, sink current = 7.72mA		0.1*VDDIO		V
		GPIO drive strength 1, sink current = 15.39mA				
		GPIO drive strength 2, sink current = 23.15mA				
		GPIO drive strength 3, sink current = 30.8mA				
VIH	Input voltage high		2			V
VIL	Input voltage low				0.8	V

6.2.3 上电时序

为确保正常的上电启动，电源、复位、Bootstrap 引脚需要满足相应的时序要求。

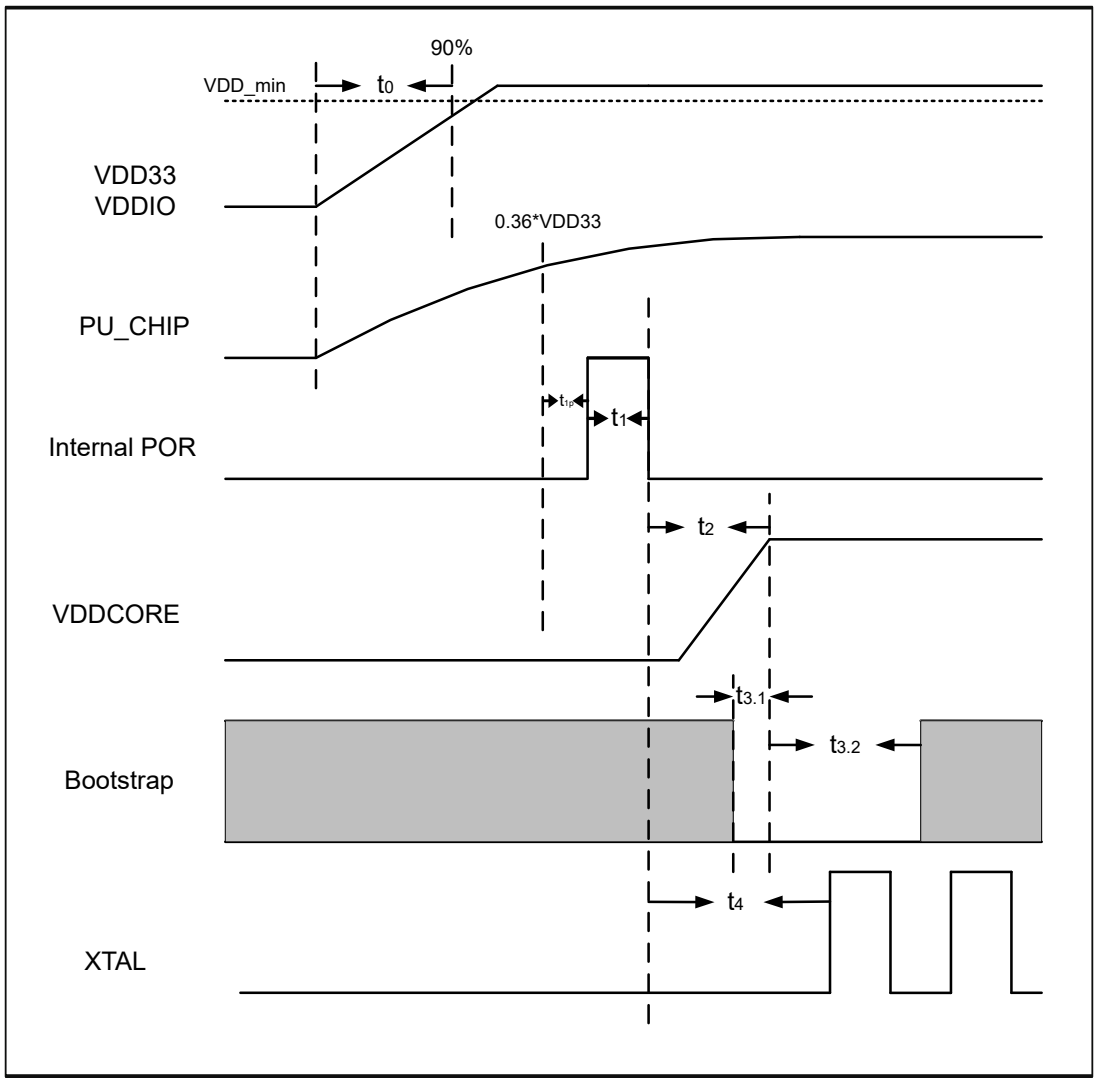

图 6.1: 上电时序

表 6.4: 上电时序参数说明

参数	说明	最小值 (ms)	典型值 (ms)	最大值 (ms)
t_0	电源电压到达 90% 的上升时间 [1]		0.1	
t_{1p}	PU_CHIP 到达阈值后，等待 POR 升高前的时间		4	
t_1	内部 POR 持续时间		3	
t_2	POR 变低到 VDDCORE 输出的时间		2	
$t_{3.1}$	Boostrap 引脚 [2]在 VDDCORE 建立前的准备时间	0		
$t_{3.2}$	Bootstrap 引脚保持有效电平的时间	2		
t_4	POR 变低到 XTAL 起振时间		3	

[1] VDD_min 是保证芯片正常工作的最小值。

[2] Bootstrap 引脚是 GPIO33。

6.2.4 复位时序

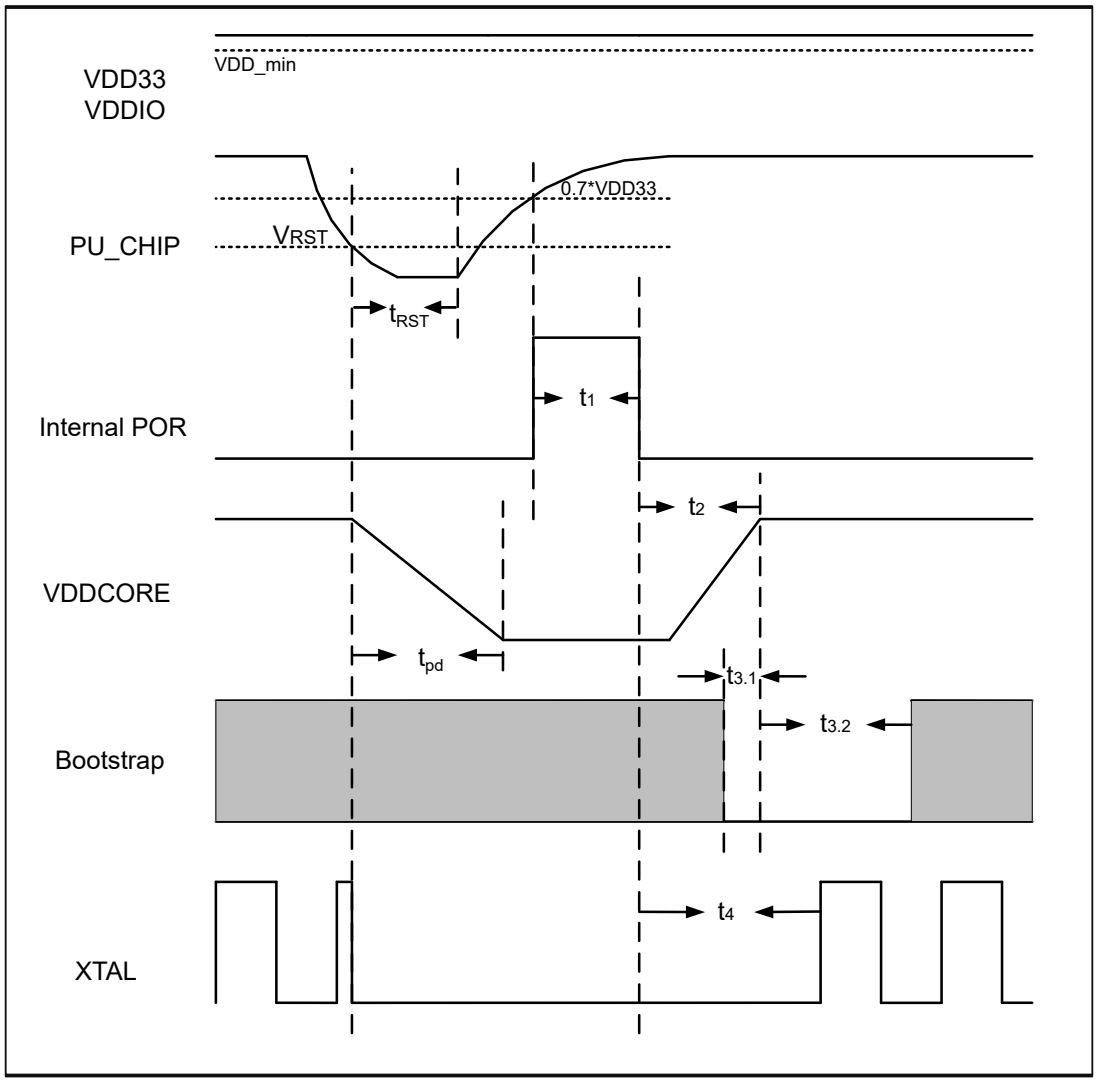

图 6.2: 复位时序

表 6.5: 复位时序参数说明

参数	说明	最小值	典型值	最大值	单位
V_{RST}	PU_CHIP 低于该值才会关机	0	0.1*VDD33	0.14*VDD33	V
t_{RST}	PU_CHIP 低于 VRST 的时间	1	1		ms

表 6.5: 复位时序参数说明 (continued)

参数	说明	最小值	典型值	最大值	单位
t_{pd}	关机后 VDDCORE 降低到 0 的时间	1	1		ms

6.2.5 温度特性

表 6.6: 温度特性

项目		最小值	典型值	最大值	单位
Ta	主芯片环境温度	-20	25	85	°C
Tj	结温度	-20		125	°C

6.2.6 通用工作条件

表 6.7: 一般操作条件

项目	描述	最小值	典型值	最大值	单位
FCPU	CPU/TCM/Cache 时钟频率		640		MHz
FBUS	系统总线时钟频率		160		MHz

6.2.7 GPADC 特性

表 6.8: ADC electrical characteristic

符号	参数	条件	最小值	典型值	最大值	单位
DNL	Differential linearity error				+/-1	LSB
INL	Integral linearity error				+/-1.5	LSB
Total error	DC measure Total error				+/-10mV	max
ENOB	Effective number of bits	12bit mode (50KHz input)		10		bit
		14bit mode (2.5KHz input)		11.4		
		16bit mode (1KHz input)		12.3		

表 6.8: ADC electrical characteristic(continued)

符号	参数	条件	最小值	典型值	最大值	单位
SNDR	Signal-to-noise distortion (PGA off)	12bit mode (50KHz input)		62		dB
		14bit mode (2.5KHz input)		72.4		
		16bit mode (1KHz input)		76.8		
SNR	Signal-to-noise ratio (PGA off)	12bit mode (50KHz input)		65.6		dB
		14bit mode (2.5KHz input)		71		
		16bit mode (1KHz input)		77.8		
SNDR	Signal-to-noise distortion (PGA gain=1)	12bit mode (50KHz input)		64		dB
		14bit mode (2.5KHz input)		69.5		
		16bit mode (1KHz input)		74		

7 产品使用

7.1 湿敏等级 (MSL)

芯片的湿敏等级为：MSL3。真空包装打开后，在 ≤30°C/60%RH 下，需要在 168 小时（7 天）内使用完毕，否则需要烘烤后上线。烘烤温度和时间可参考 IPC/JEDECJ-STD-033B01。

表 7.1: Reference Conditions for Drying Mounted or Unmounted SMD Packages (User Bake: Floor life begins counting at time = 0 after bake)

Package Body	Level	Bake @ 125°C		Bake @ 90°C ≤5% RH		Bake @ 40°C ≤5% RH	
		Exceeding Floor Life by >72 h	Exceeding Floor Life by ≤72 h	Exceeding Floor Life by >72 h	Exceeding Floor Life by ≤72 h	Exceeding Floor Life by >72 h	Exceeding Floor Life by ≤72 h
Thickness ≤1.4 mm	2	5 hours	3 hours	17 hours	11 hours	8 days	5 days
	2a	7 hours	5 hours	23 hours	13 hours	9 days	7 days
	3	9 hours	7 hours	33 hours	23 hours	13 days	9 days
	4	11 hours	7 hours	37 hours	23 hours	15 days	9 days
	5	12 hours	7 hours	41 hours	24 hours	17 days	10 days
	5a	16 hours	10 hours	54 hours	24 hours	22 days	10 days

7.2 静电放电（ESD）

- 人体放电模式 (HBM): 2000V
- 组件充电模式 (CDM): 500V

7.3 回流焊接曲线 (Reflow Profile)

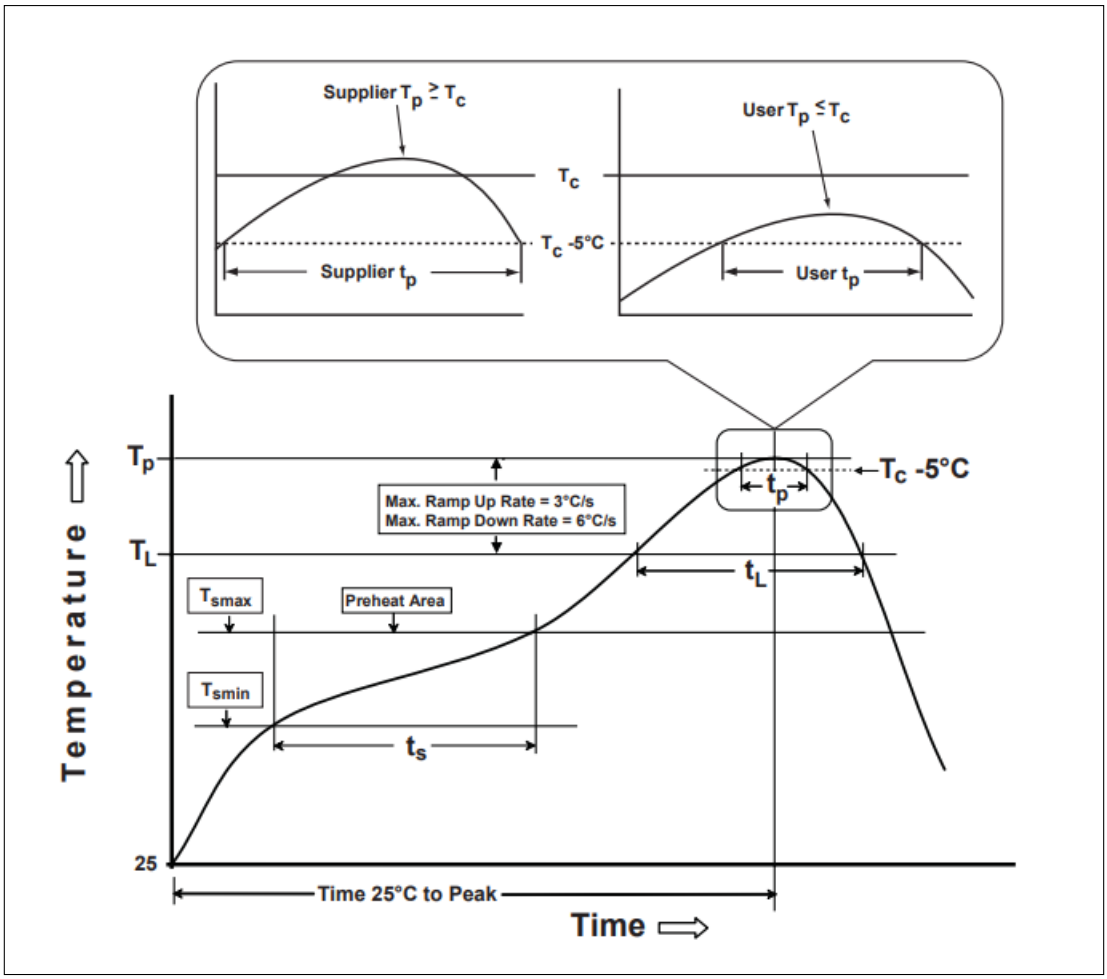

图 7.1: Classification Profile (Not to scale)

表 7.2: Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat/Soak Temperature Min (T_{smin}) Temperature Max (T_{smax}) Time (t_s) from ($T_{smin}$to T_{smax})	 100 °C 150 °C 60-120 seconds	 150 °C 200 °C 60-120 seconds
Ramp-up rate (T_L to T_p)	3 °C/second max.	3 °C/second max.

表 7.2: Classification Reflow Profiles(continued)

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Liquidous temperature (T_L) Time (t_L) maintained above T_L	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body temperature (T_p)	240 °C+0/-5 °C	250 °C+0/-5 °C
Time (t_p)* within 5 °C of the specified classification temperature (T_c)	10-30 seconds	20-40 seconds
Ramp-down rate ($T_p$to T_L)	6 °C/second max	6 °C/second max
Time 25 °C to peak temperature	6 minutes max	8 minutes max
- Tolerance for peak profile temperature (Tp) is defined as a supplier minimum and a user maximum.		

具体可参考 IPC/JEDEC J-STD-020E。

8 参考设计

9 封装信息 QFN56

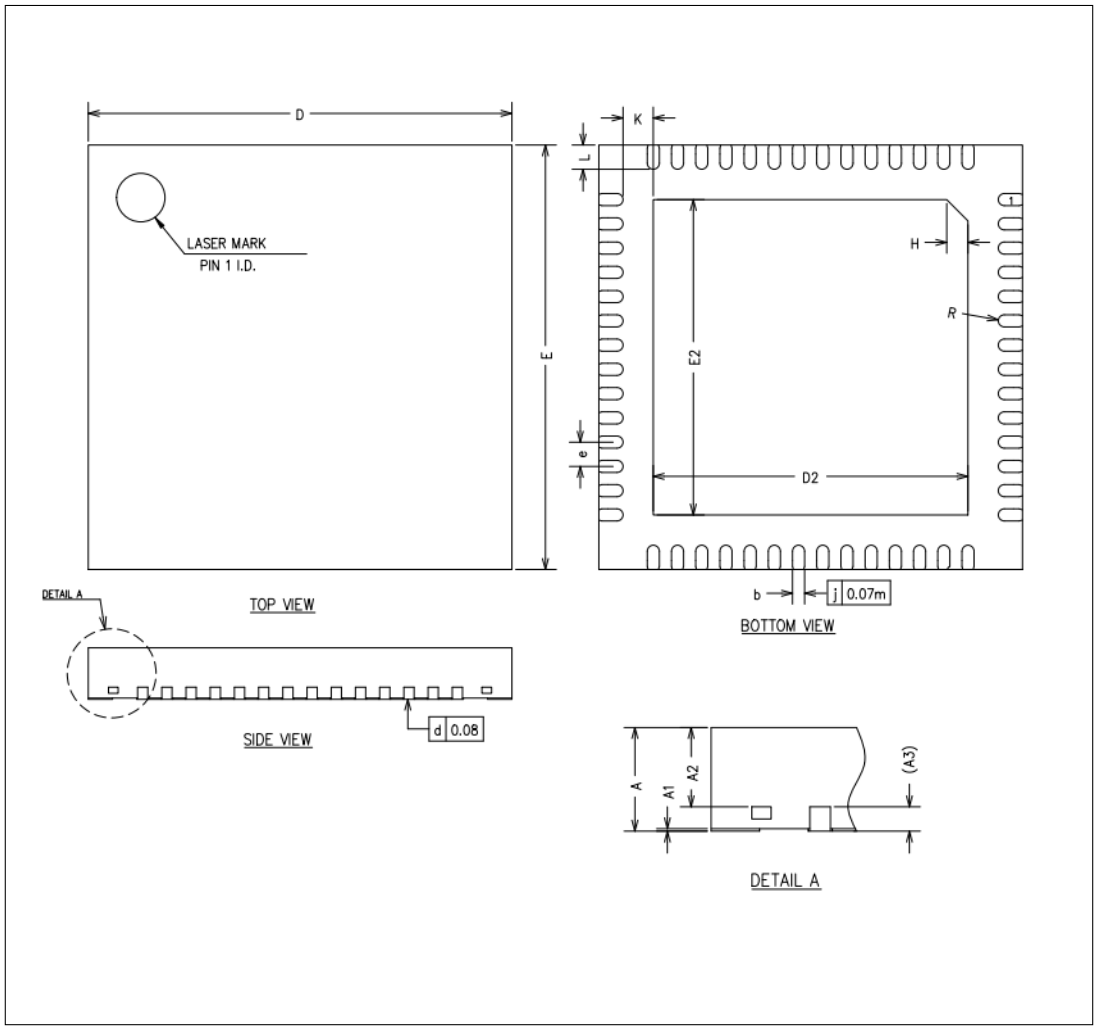

图 9.1: QFN56 封装图

表 9.1: QFN56 尺寸说明

标号	测量单位：毫米		
	最小值	典型值	最大值
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A2	0.60	0.65	0.70
A3	0.20 REF		
b	0.15	0.20	0.25

表 9.1: QFN56 尺寸说明 (continued)

标号	测量单位：毫米		
	最小值	典型值	最大值
D	6.90	7.00	7.10
E	6.90	7.00	7.10
D2	5.10	5.20	5.30
E2	5.10	5.20	5.30
e	0.30	0.40	0.50
H	0.35 REF		
K	0.50 REF		
L	0.35	0.40	0.45
R	0.09	-	-

10 封装信息 QFN68

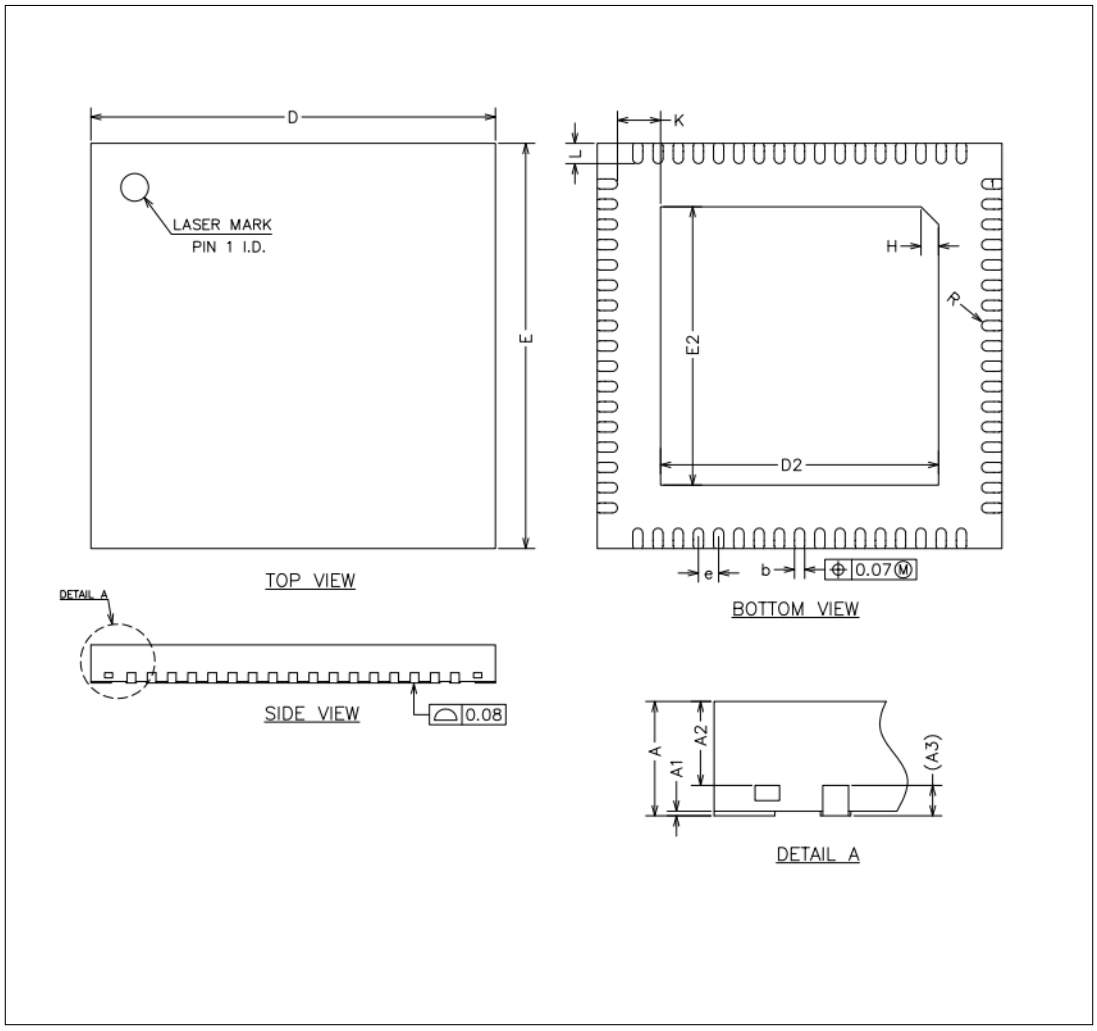

图 10.1: QFN68 封装图

表 10.1: QFN68 尺寸说明

符号	测量单位：毫米		
	最小值	典型值	最大值
A	0.85	0.90	0.95
A1	0.00	0.02	0.05
A2	0.65	0.70	0.75
A3	0.20 REF		
b	0.15	0.20	0.25

表 10.1: QFN68 尺寸说明 (continued)

符号	测量单位：毫米		
	最小值	典型值	最大值
D	7.90	8.00	8.10
E	7.90	8.00	8.10
D2	5.40	5.50	5.60
E2	5.40	5.50	5.60
e	0.30	0.40	0.50
H	0.35 REF		
K	0.70	-	-
L	0.30	0.40	0.50
R	0.09	-	-

11 标志定义

12 订购信息

13 版本信息

表 13.1: 修改记录

日期	版本	修改内容
2025/3/8	0.9	初版
2025/6/9	0.9.1	1. 修改管脚定义 2. 增加 CAN 的描述
2025/10/10	0.9.2	1. 增加 TOUCH 和 MiPi DSI 的描述 2. 更新 CAN 的介绍
2026/4/7	0.9.3	1. 增加 QFN56 的描述
2026/4/21	0.9.4	1. 修改 I2C/CAN/PWM/TOUCH/AUADC/PEC 的 pinmux 功能