

BL702L/704L

Datasheet

Version: 2.1

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Features

- Wireless
  - 2.4 GHz RF transceiver
  - Bluetooth Low Energy 5.3
  - Zigbee 3.0
  - Thread / Matter
  - BLE/Zigbee/Thread/Three-line Wi-Fi coexistence
  - Integrated TRSW/PA/LNA
- Microcontroller
  - 32-bit RISC CPU
  - L1 cache
  - RTC timer update to one year
  - Two 32-bit general purpose timers
  - Four DMA channels
  - DFS from 1MHz to 128MHz
  - JTAG development support
  - XIP QSPI Flash/pSRAM support
- Memory
  - 100KB RAM
    - 16KB cache (available for regular RAM)
    - 80KB OCRAM
    - 4KB HBN RAM
  - 256KB ROM
  - 1Kb eFuse
  - Embedded Flash (Optional)
  - Embedded pSRAM (Optional)
- Security
  - Secure boot
  - Secure debug ports
  - AES 128
  - SHA-1/256
  - TRNG (True Random Number Generator)
  - PKA (Public Key Accelerator)
- Peripherals
  - One SPI master/slave
  - One UART
  - One I2C, support host mode
  - Five PWM channels
  - Key-Scan interface
  - 12-bit general ADC
  - Audio ADC
  - High precision ADC
  - IR remote(TX)
  - Up to 29 GPIOs (configurable functions)
- Power Modes(Ultra-low Power modes)
  - Active (Normal/Rx/Tx)
  - Idle mode
  - Power Down Sleep
  - Hibernate
  - Off
- Clock
  - Support XTAL (mainly 32MHz)
  - Internal RC 32KHz oscillator

- Internal RC 32MHz oscillator
- Support XTAL (mainly 32KHz)
- Internal System DLL

- Package Type
  - 32 pin QFN
  - 40 pin QFN

Contents

1 Overview . . . 9
2 Functional Description . . . 10
2.1 CPU . . . 10
2.2 Cache . . . 11
2.3 Memory . . . 11
2.4 DMA . . . 11
2.5 Memory Map . . . 11
2.5.1 Mutual conversion between TCM and Cache RAM resources . . . 12
2.6 Interrupt . . . 12
2.7 Boot . . . 13
2.8 Power . . . 13
2.9 Clock . . . 13
2.10 Peripheral . . . 13
2.10.1 GPIO . . . 13
2.10.2 UART . . . 14
2.10.3 SPI . . . 14
2.10.4 I2C . . . 14
2.10.5 TIMER . . . 15
2.10.6 PWM_V1 . . . 15
2.10.7 PWM_V2 . . . 15
2.10.8 IR(IR-remote) . . . 16
2.10.9 GPADC . . . 16
2.10.10 Audio ADC . . . 16
2.10.11 High precision ADC . . . 17
2.10.12 Debug interface . . . 17

3 Pin Definition . . . 18
3.1 GPIO initial state . . . 27
4 RF Characteristsic . . . 30
5 Power Consumption . . . 32
6 Electrical Specifications . . . 33
6.1 Absolute Maximum Rating . . . 33
6.2 Operating Condition . . . 33
6.2.1 Power characteristics . . . 33
6.2.2 IO DC characteristics . . . 33
6.2.3 Power-on sequence . . . 34
6.2.4 Shutdown Sequence . . . 36
6.2.5 Temperature characteristics . . . 37
6.2.6 General operating conditions . . . 37
6.2.7 GPADC characteristics . . . 37
7 Product use . . . 39
7.1 Moisture Sensitivity Level(MSL) . . . 39
7.2 Electro-Static discharge（ESD） . . . 40
7.3 Reflow Profile . . . 40
8 Reference Design . . . 42
9 Package Information(QFN32) . . . 43
10 Package Information(QFN40) . . . 45
11 Top Marking Definition . . . 47
12 Ordering Information . . . 48
13 Revision history . . . 50

List of Figures

1.1 Block Diagram 9

2.1 System Architecture 10

3.1 BL702L 32-pin layout 18
3.2 BL704L 40-pin layout 19

6.1 Power-on sequence 35
6.2 Shutdown sequence 36

7.1 Classification Profile (Not to scale) 40

9.1 QFN32 Package drawing 43

10.1 QFN40 Package drawing 45

11.1 Top Marking Definition 47

12.1 Part Number 48

List of Tables

2.1 Memory Map . . . 11
2.2 WayDisable settings . . . 12
2.3 Boot mode . . . 13

3.1 Pin definition . . . 19
3.2 BL702L GPIO initial state . . . 27
3.3 BL704L GPIO initial state . . . 28

4.1 BLE RX RF characteristics . . . 30
4.2 BLE TX RF characteristics . . . 30
4.3 ZigBee RX RF characteristics . . . 31
4.4 ZigBee TX RF characteristics . . . 31

5.1 Power Modes & Whole-chip Current . . . 32

6.1 Absolute Maximum Rating . . . 33
6.2 Recommended Power Operating Range . . . 33
6.3 IO DC characteristics . . . 34
6.4 Power-on sequence parameters . . . 35
6.5 Shutdown sequence parameters . . . 36
6.6 Recommended Temperature Operating Range . . . 37
6.7 General Operating Conditions . . . 37
6.8 GPADC characteristics . . . 37
6.9 ADC electrical characteristic . . . 38

7.1 Reference Conditions for Drying Mounted or Unmounted SMD Packages (User Bake: Floor life begins counting at time = 0 after bake) . . . 39
7.2 Classification Reflow Profiles . . . 41

9.1 QFN32 Size Description . . . 44

10.1 QFN40 Size Description 45

12.1 Part Order Options 48
12.2 Product Packaging Information 49

13.1 Document revision history 50

1 Overview

BL702L/704L is a highly integrated 802.15.4 (Zigbee/Thread/Matter) and BLE combo chipset for IoT applications.

Wireless subsystem contains 2.4G radio, 802.15.4 + BLE baseband and MAC designs. Microcontroller subsystem contains 32-bit RISC CPU, high-speed cache and memories. Power Management Unit controls ultralow-power modes. Moreover, variety of security features are supported.

Peripheral interfaces include SPI, UART, I2C, PWM, KeyScan, GPADC, Audio ADC, IR remote(TX) and GPIO.

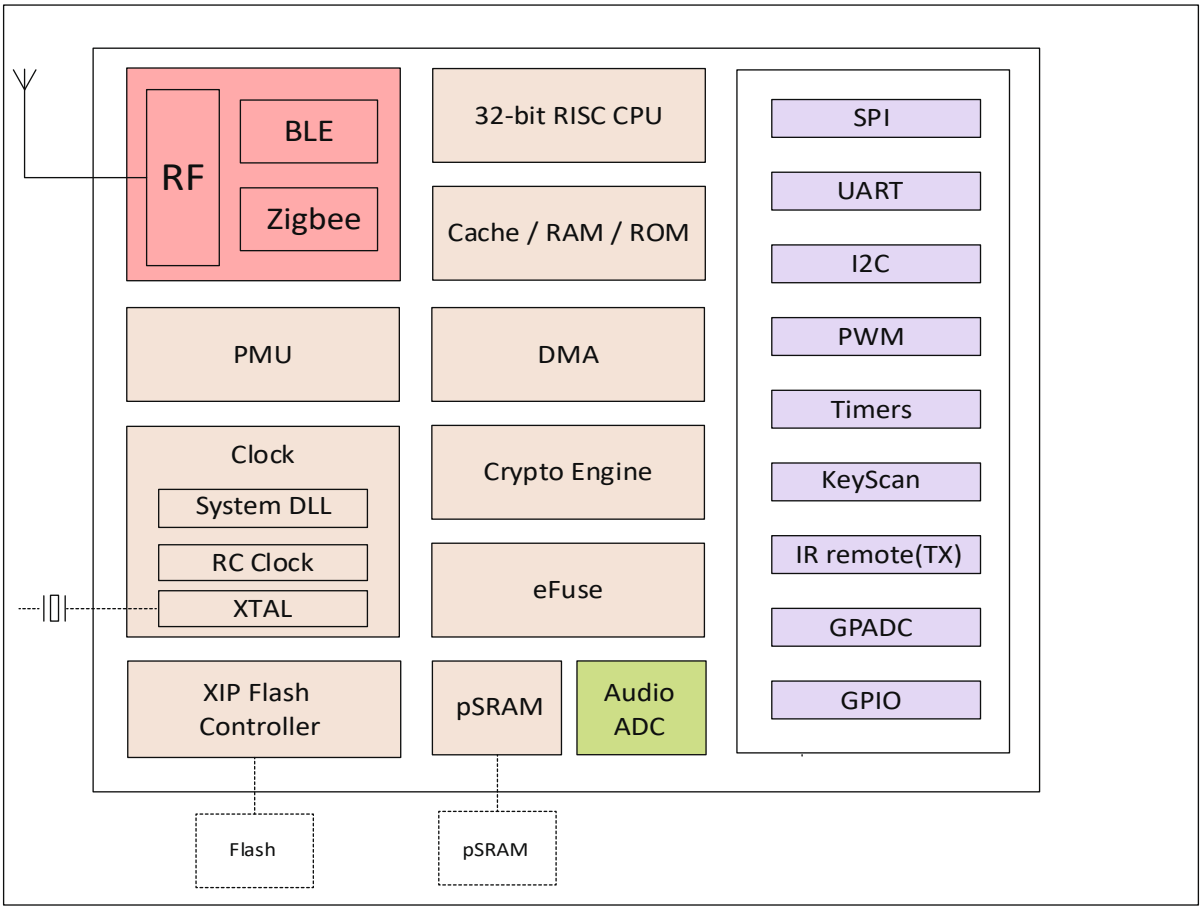


Fig. 1.1: Block Diagram

2 Functional Description

BL702L/704L main functions described as follows:

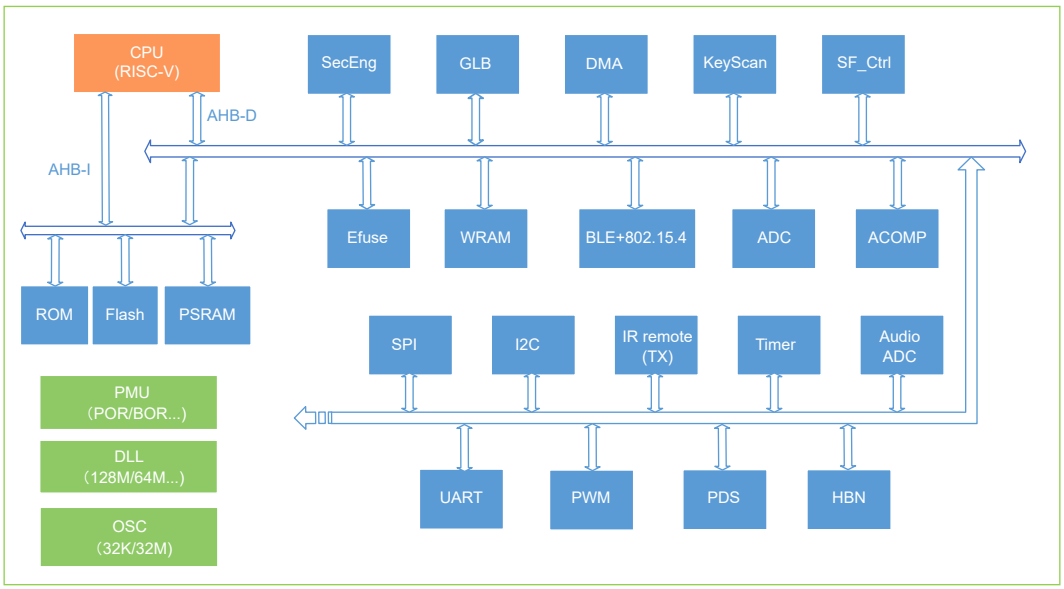


Fig. 2.1: System Architecture

2.1 CPU

BL702L/704L 32-bit RISC CPU contains FPU (floating-point unit) for 32-bit single-precision arithmetic, three-stage pipelined (IF, EXE, WB), compressed 16 and 32-bit instruction set, standard JTAG debugger port including 4 hardware-programmable breakpoints, interrupt controller including 64 interrupts and 16 interrupt levels/priorities for low latency interrupt processing. Up to 128MHz clock frequency, can be dynamically configured to change clock frequency, enter the power saving mode to achieve low power consumption.

Both zigbee/BLE stack and application run on single 32-bit RISC CPU for simple and ultra-low power applications. CPU performance 2.92 CoreMark / MHz.

2.2 Cache

BL702L/704L cache improves CPU performance to access external memory. Cache memories can be partially or fully configured as TCM (tightly coupled memory).

2.3 Memory

BL702L/704L memory includes: on-chip zero-delay SRAM memory, read-only memory, write-once memory, Embedded flash (optional), embedded pSRAM (optional).

2.4 DMA

The DMA controller has 4 dedicated channels to manage data transfers between peripherals and memory to improve CPU/bus efficiency. DMA has four transfer types, memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral modes.

The DMA also supports the LLI (Linked List Item) feature, which consists of a series of linked lists that predefine multiple transfers, and then the hardware automatically completes all transfers based on the size and address of each LLI.

Peripherals supported by DMA include UART, I2C, SPI, IR(TX) and GPADC。

2.5 Memory Map

Table 2.1: Memory Map

Module	Target	Base Address	Size	Description
FLASH	Flash	0x23000000	16MB	Application address space
OCRAM	OCRAM	0x22020000	80KB	On-chip memory
PSRAM	pSRAM	0x24000000	16MB	pSRAM memory address space (optional, depends on the specific chip model)
RAM	HBN RAM	0x20010000	4KB	HBN RAM,mainly used for data saving in ultra-low power mode
Peripheral	HBN	0x4000F000	2KB	Hibernate register
	PDS	0x4000E000	4KB	Power-down sleep register
	DMA	0x4000C000	4KB	DMA control register
	SF_Ctrl	0x4000B000	4KB	Serial flash control register
	Audio ADC	0x4000AD00	256B	Audio ADC control register
	IRR	0x4000A600	256B	IR remote control register
	TIMER	0x4000A500	256B	TIMER control register
	PWM	0x4000A400	256B	PWM control register
	I2C	0x4000A300	256B	I2C control register
	SPI	0x4000A200	256B	SPI control register

Table 2.1: Memory Map(continued)

Module	Target	Base Address	Size	Description
	UART	0x4000A000	256B	UART control register
	L1C	0x40009000	4KB	L1C control register
	Efuse	0x40007000	4KB	Efuse storage control register
	TZ	0x40005000	4KB	TrustZone control register
	SEC_ENG	0x40004000	4KB	Security engine control register
	GPIP	0x40002000	1KB	General purpose ADC interface control register
	GLB	0x40000000	4KB	Global control register
ROM	ROM	0x21000000	256KB	Bootrom address space

2.5.1 Mutual conversion between TCM and Cache RAM resources

To increase memory usage efficiency, it is possible to allocate all or part of the 16K RAM of the Cache to the TCM space, so that users can adjust the memory usage and efficiency according to the actual situation. The maximum Cache can be set to 16K, divided into 4 ways, each way is 4K, and the unit of adjustment is 1 way, which is 4K. The default size of ITCM is 16K. The actual space size of Cache and ITCM can be flexibly adjusted.

Table 2.2: WayDisable settings

WayDisable	Cache	ITCM	ITCM Address
none	16K	0K	none
one way	12K	4K	0x2201F000
two way	8K	8K	0x2201E000
three way	4K	12K	0x2201D000
four way	0K	16K	0x2201C000

2.6 Interrupt

BL702L/704L supports internal RTC clock wake-up and external interrupt wake-up to realize low-power sleep wake-up function.

The CPU interrupt controller supports a total of 64 maskable interrupt trigger sources including UART interrupt, I2C interrupt, SPI interrupt, timer interrupt, DMA interrupt, etc.

All I/O pins can be configured as external interrupt input mode, the external interrupt supports nine trigger types: synchronous high/low level trigger, synchronous rising/falling edge trigger, asynchronous high/low level trigger, asynchronous rising edge /Falling edge trigger and synchronous double edge trigger.

2.7 Boot

BL702L/704L supports multiple boot options: UART, Flash.

Table 2.3: Boot mode

Boot pin	Level	Description
GPIO16	1	Boot from UART(GPIO14/15), this mode is mainly used for flash programming or downloading image to RAM for execution (wireless transparent transmission scenario)
	0	Launch application image from Flash

2.8 Power

PMU (power management unit) manages the power of the entire chip and is divided into running, idle, sleep, hibernation and power off modes. The software can be configured to enter sleep mode and wake-up via RTC timer or EINT to achieve low-power sleep and accurate wake-up management.

Power down sleep modes are flexible for applications to configure as the lowest power consumption.

2.9 Clock

Clock control unit generates clocks to the core MCU and the peripheral SOC devices. The root clock source can be XTAL, DLL or RC oscillator. Dynamic power-saved by proper configurations such as sel, div, en, etc. PMU runs at 32KHz clock to keep system low-power in sleep mode.

2.10 Peripheral

Peripherals include IR-remote, SPI, UART, I2C, PWM, Timer, KeyScan, Audio ADC and GPADC.

2.10.1 GPIO

The BL702L has 22 GPIOs and the BL704L has 29 GPIOs with the following features:

- Each GPIO can be used as general-purpose input and output function, pull-up/pull-down/float can be configured by software
- Each GPIO supports interrupt function, the interrupt supports synchronous high/low level trigger, synchronous rising/falling edge trigger, asynchronous high/low level trigger, asynchronous rising/falling edge trigger and synchronous double edge trigger
- Each GPIO can be set to high-impedance state for low-power modes
- Each GPIO can control the output state through the Set/Clear register

2.10.2 UART

The chip has one built-in universal asynchronous serial transceivers with the following features:

- Supports CTS and RTS flow control in hardware
- Support LIN master/slave function
- Support RS-485 function
- Configurable data bits, stop bits and parity bits
- Supports automatic baud rate detection for common/fixed characters
- The working clock can be selected as FCLK, XCLK or 64MHz, the maximum baud rate supports 8Mbps
- TX and RX have independent FIFO, FIFO depth is 16 bytes, support DMA function

2.10.3 SPI

The chip has a built-in SPI, which can be configured as master mode or slave mode. The SPI module clock is XCLK or BCLK, and has the following characteristics:

- In master mode, clock frequency up to 32 MHz
- In slave mode, the maximum allowed master clock frequency is 32 MHz
- The bit width of each frame can be configured as 8-bit / 16-bit / 24-bit / 32-bit
- Adaptive FIFO depth change characteristics, suitable for high-performance scene applications
  - When the bit width is 32 bits, the depth of the FIFO is 4
  - When the bit width is 24 bits, the depth of the FIFO is 4
  - When the bit width is 16 bits, the depth of the FIFO is 8
  - When the bit width is 8 bits, the depth of the FIFO is 16
- Support DMA transfer mode

2.10.4 I2C

The chip has one built-in I2C interfaces with the following features:

- Supports multi-master mode and arbitration function
- The working clock can be selected as BCLK or XCLK
- With device address register, register address register, register address length can be set to 1 byte/ 2 bytes/ 3 bytes/ 4 bytes
- I2C has independent transceiver FIFO, FIFO depth is 2 word

- Supports 10-bit address mode
- Support DMA function

2.10.5 TIMER

The chip has two built-in 32-bit general-purpose timers and a watchdog timer with the following features:

- The clock source of the general timer can be selected from XTAL/32K/1K, and the clock source of the watchdog timer can be selected from XTAL/32K/1K/BCLK
- 8-bit divider for each counter
- Each group of general-purpose timers includes three compare registers, supports compare interrupts, and supports FreeRun mode and PreLoad mode in counting mode
- 16-bit watchdog timer, supports two watchdog overflow modes: interrupt or reset

2.10.6 PWM_V1

The chip has a built-in PWM V1 module PWM0_CH0 with the following features:

- Three clock sources BCLK/XCLK/32K selectable with 16-bit clock divider
- 16-bit period value setting
- Dual threshold settings for flexible PWM duty cycle and phase settings to increase pulse flexibility
- PWM output signal can be set to flip or not
- Support cycle number interrupt

2.10.7 PWM_V2

The chip has a built-in V2 version of the PWM module, including 4-channel PWM signal output PWM1_CH0-PWM1_CH3, with the following characteristics:

- Three clock sources BCLK/XCLK/32K selectable with 16-bit clock divider
- 16-bit period value setting
- Independent dual threshold settings for each PWM channel, allowing different duty cycles and phases to be set for increased pulse flexibility
- Each PWM output pin can be set to a different active level
- Each PWM channel has a separate connection switch to select whether to connect to the internal counter or not, and to set the default output level when not connected
- Software brake signal to set the PWM output level to a predefined state

- Up to 9 trigger sources for triggering ADC conversions
- Supports 10 types of interrupts: counter overflow interrupt, threshold comparison interrupt, cycle count interrupt, etc

2.10.8 IR(IR-remote)

The chip has a built-in IR remote control (TX only) with the following features.

- Operating clock is XCLK
- Supports sending data in fixed protocol NEC, RC-5, and pulse width counting in any format
- Supports adjustable carrier frequency and duty cycle
- Continuous transmit mode for sending large amount of data at one time
- Support DMA function

2.10.9 GPADC

The chip has a built-in 12bits successive approximation analog-to-digital converter (ADC) with the following features.

- The maximum sampling rate of single-channel continuous conversion mode can reach 2M, and the maximum sampling rate of other conversion modes is 500K
- Supports 12 external analog inputs and several internal analog signal options
- Support single-channel single conversion, single-channel continuous conversion, multi-channel single conversion, multi-channel continuous conversion
- Supports 2.0V, 3.2V selectable internal reference voltages and 12/14/16bits (via oversampling) left-aligned conversion results
- 32-byte deep FIFO, multiple interrupt support, DMA support
- ADC can be used to measure supply voltages in addition to common analog signal measurements
- Can be used for temperature detection by measuring internal/external diode voltages

2.10.10 Audio ADC

- The chip has an integrated 1-channel audio ADC (not to be used simultaneously with the high precision ADC) with the following features:
  - Sampling rate:8k~96k
  - Signal-to-noise ratio (A-W): 96dB @ 6dB gain, 48K sampling rate
  - Harmonic distortion + noise: -90dB @ 6dB gain, 48K sample rate

  - Analogue preamp gain: 6 to 42 dB, 3dB steps
  - Analogue fully differential input or single-ended input
- Adjustable high-pass filter and digital volume control
- PDM interface support (1 way DMIC supported)
- Input signal multiplexing GPIO
- Transmit FIFO width of 32-bit, depth of 8
- Support for DMA transfer mode

2.10.11 High precision ADC

- The chip has a built-in 1-channel high precision ADC (not to be used simultaneously with audio codec) with the following features.
  - Supports fully differential input, 4 channels
  - Effective resolution (ER): 19.5 bit
  - Programmable gain amplifier: 6dB to 42dB (2 to 128x), 3dB steps
  - Programmable data rates: 20SPS, 100SPS, 200SPS, 400SPS, 1000SPS, 2000SPS
  - Supports high accuracy/low latency dual set digital filters
  - Supports 50Hz/60Hz simultaneous frequency suppression
  - Supports software global chopping, ER=20.7bit, below 1uV detuning voltage
- Multiplexed GPIO input signals
- Transmit FIFO width of 32-bit, depth of 8
- Supports polling, interrupt and DMA transfer modes

2.10.12 Debug interface

Support standard JTAG 4-wire debug interface, support debugging using Jlink/OpenOCD/CK Link and other debuggers.

3 Pin Definition

BL702L 32-pin package includes 6 fixed power ports, 4 fixed analog ports, and up to 22 configurable GPIO ports.

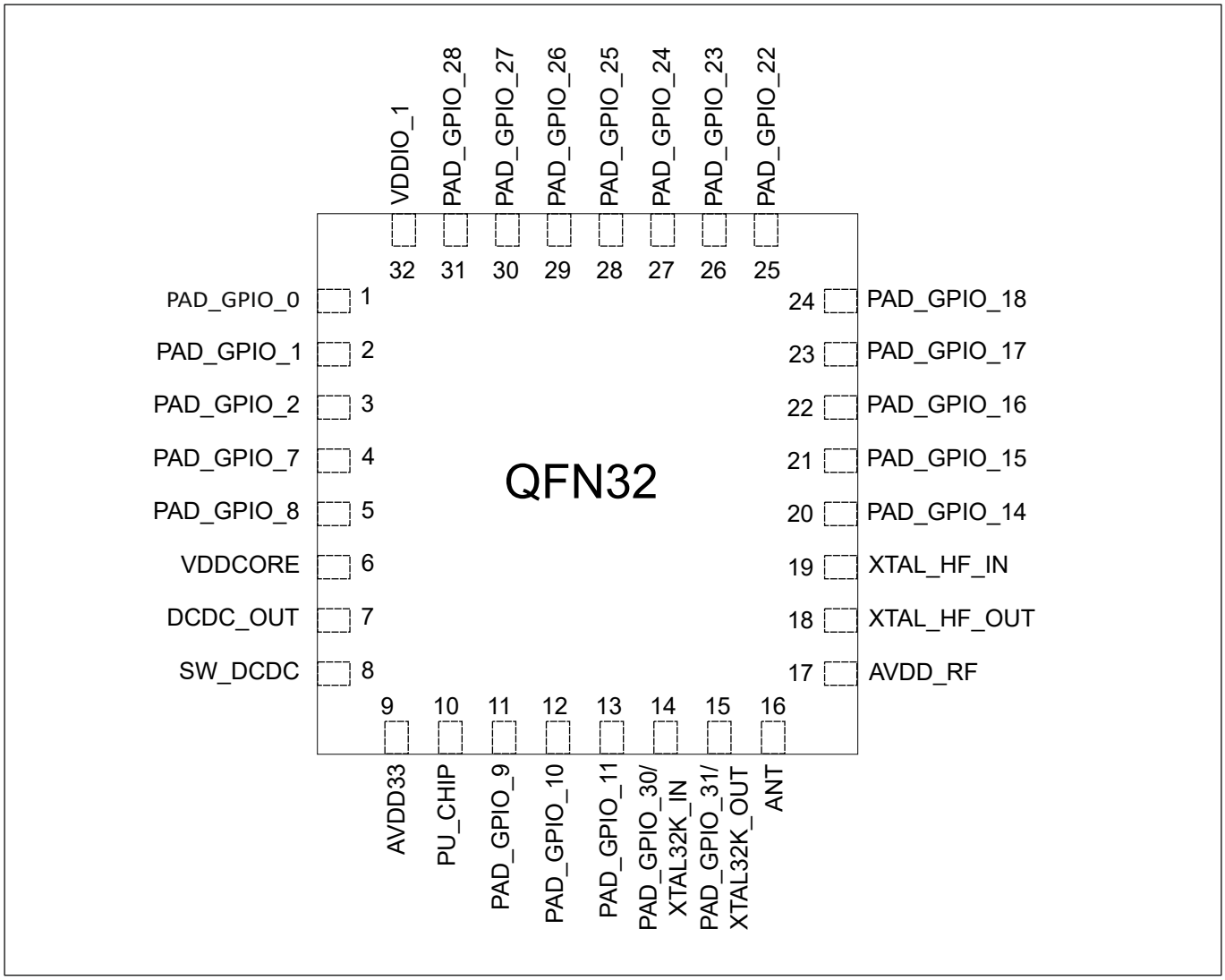


Fig. 3.1: BL702L 32-pin layout

BL704L 40-pin package includes 7 fixed power ports, 4 fixed analog ports, and up to 29 configurable GPIO ports.

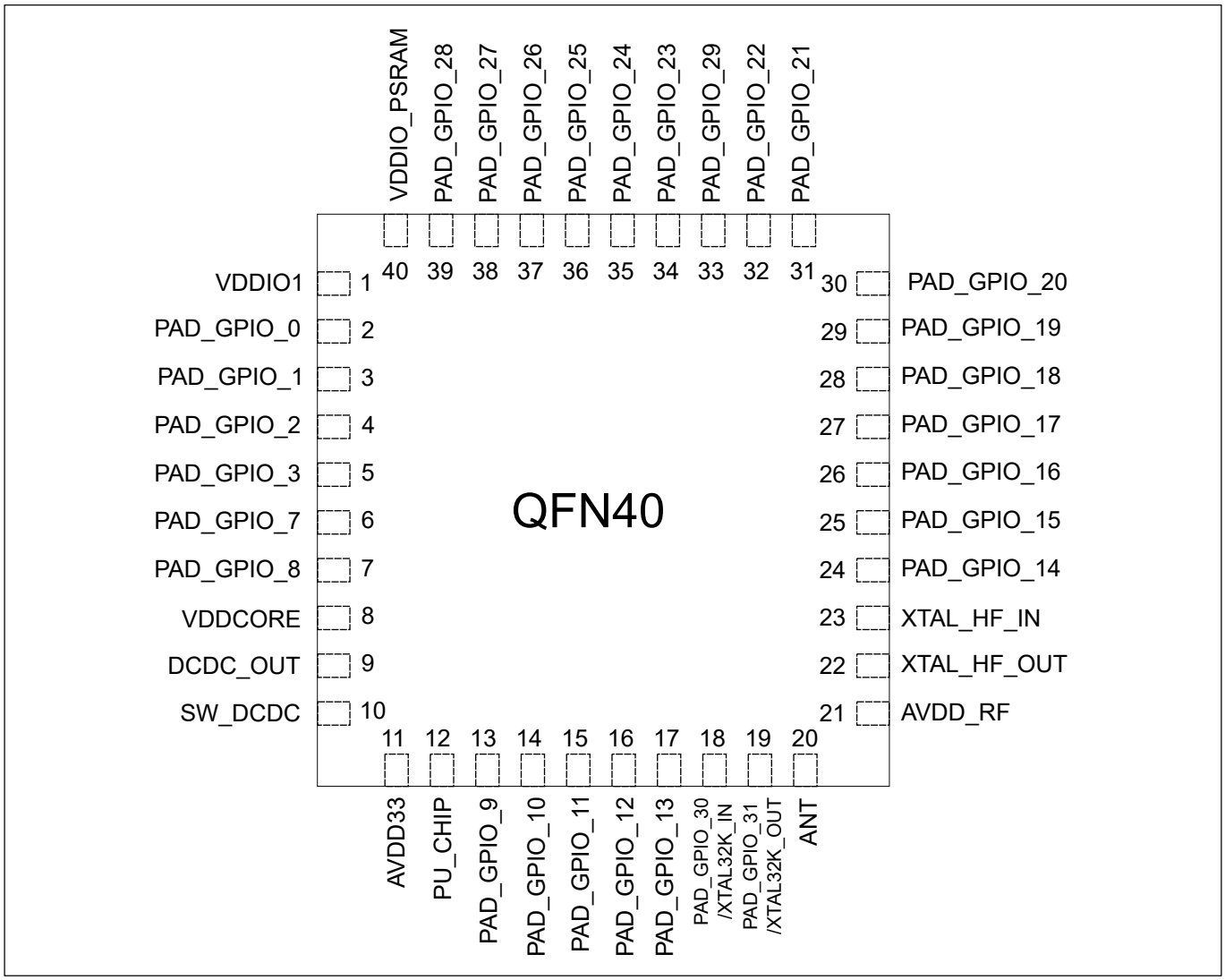


Fig. 3.2: BL704L 40-pin layout

Table 3.1: Pin definition

QFN32	QFN40	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
1	2	VDDIO_1	DI/DO	PAD_GPIO_0	2	-	-	-
					4	-	SPI_MOSI [1]	SPI_MOSI
					5	-	PDM_CLK_O	PDM_CLK_O
					6	-	I2C_SCL	I2C_SCL
					7	uart_sig_0_sel=0	UART0_RTS	UART0_RTS
						uart_sig_0_sel=1	UART0_CTS	UART0_CTS
						uart_sig_0_sel=2	UART0_TXD	UART0_TXD
						uart_sig_0_sel=3	UART0_RXD	UART0_RXD
					8	-	PWM0_CH0	PWM0_CH0
					10	-	-	-
					11	-	SWGPIO0	SWGPIO0
					14	-	TMS	TMS
					21	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					22	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O

Table 3.1: Pin definition(continued)

QFN32	QFN40	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
2	3	VDDIO_1	DI/DO	PAD_GPIO_1	2	-	-	-
					4	-	SPI_MISO	SPI_MISO
					5	-	PDM_0_IN	PDM_0_IN
					6	-	I2C_SDA	I2C_SDA
					7	uart_sig_1_sel=0	UART0_RTS	UART0_RTS
						uart_sig_1_sel=1	UART0_CTS	UART0_CTS
						uart_sig_1_sel=2	UART0_TXD	UART0_TXD
						uart_sig_1_sel=3	UART0_RXD	UART0_RXD
					8	-	PWM1_CH0	PWM1_CH0
					10	-	-	-
					11	-	SWGPIO1	SWGPIO1
					14	-	TDI	TDI
					21	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					22	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
3	4	VDDIO_1	DI/DO	PAD_GPIO_2	2	-	-	-
					4	-	SPI_SS	SPI_SS
					5	-	PDM_CLK_O	PDM_CLK_O
					6	-	I2C_SCL	I2C_SCL
					7	uart_sig_2_sel=0	UART0_RTS	UART0_RTS
						uart_sig_2_sel=1	UART0_CTS	UART0_CTS
						uart_sig_2_sel=2	UART0_TXD	UART0_TXD
						uart_sig_2_sel=3	UART0_RXD	UART0_RXD
					8	-	PWM1_CH1	PWM1_CH1
					10	-	AUADC_CH0	AUADC_CH0
					11	-	SWGPIO2	SWGPIO2
					14	-	TCK	TCK
					21	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					22	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
-	5	VDDIO_1	DI/DO	PAD_GPIO_3	2	-	-	-
					4	-	SPI_SCLK	SPI_SCLK
					5	-	PDM_0_IN	PDM_0_IN
					6	-	I2C_SDA	I2C_SDA
					7	uart_sig_3_sel=0	UART0_RTS	UART0_RTS
						uart_sig_3_sel=1	UART0_CTS	UART0_CTS
						uart_sig_3_sel=2	UART0_TXD	UART0_TXD
						uart_sig_3_sel=3	UART0_RXD	UART0_RXD
					8	-	PWM1_CH2	PWM1_CH2
					10	-	AUADC_CH1	AUADC_CH1
					11	-	SWGPIO3	SWGPIO3
					14	-	TDO	TDO
					21	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					22	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
4	6	VDDIO_1	DI/DO	PAD_GPIO_7	2	-	-	-
					4	-	SPI_SCLK	SPI_SCLK
					5	-	PDM_0_IN	PDM_0_IN
					6	-	I2C_SDA	I2C_SDA
					7	uart_sig_3_sel=0	UART0_RTS	UART0_RTS
						uart_sig_3_sel=1	UART0_CTS	UART0_CTS
						uart_sig_3_sel=2	UART0_TXD	UART0_TXD
						uart_sig_3_sel=3	UART0_RXD	UART0_RXD
					8	-	PWM1_CH1	PWM1_CH1
					10	-	ADC_CH7/AUADC_CH2	ADC_CH7/AUADC_CH2
					11	-	SWGPIO7	SWGPIO7
					14	-	TDO	TDO
					21	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					22	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O

Table 3.1: Pin definition(continued)

QFN32	QFN40	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
5	7	VDDIO_1	DI/DO	PAD_GPIO_8	2	-	-	-
					4	-	SPI_MOSI	SPI_MOSI
					5	-	PDM_CLK_O	PDM_CLK_O
					6	-	I2C_SCL	I2C_SCL
					7	uart_sig_0_sel=0	UART0_RTS	UART0_RTS
						uart_sig_0_sel=1	UART0_CTS	UART0_CTS
						uart_sig_0_sel=2	UART0_TXD	UART0_TXD
						uart_sig_0_sel=3	UART0_RXD	UART0_RXD
					8	-	PWM1_CH2	PWM1_CH2
					10	-	ADC_CH8/AUADC_CH3	ADC_CH8/AUADC_CH3
					11	-	SWGPIO8	SWGPIO8
					14	-	TMS	TMS
					21	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					22	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
11	13	AVDD33	DI/DO	PAD_GPIO_9	2	-	-	-
					4	-	SPI_MISO	SPI_MISO
					5	-	-	-
					6	-	I2C_SDA	I2C_SDA
					7	uart_sig_1_sel=0	UART0_RTS	UART0_RTS
						uart_sig_1_sel=1	UART0_CTS	UART0_CTS
						uart_sig_1_sel=2	UART0_TXD	UART0_TXD
						uart_sig_1_sel=3	UART0_RXD	UART0_RXD
					8	-	PWM1_CH3	PWM1_CH3
					10	-	ADC_CH9	ADC_CH9
					11	-	SWGPIO9	SWGPIO9
					14	-	TDI	TDI
					21	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					22	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
12	14	AVDD33	DI/DO	PAD_GPIO_10	2	-	-	-
					4	-	SPI_SS	SPI_SS
					5	-	-	-
					6	-	I2C_SCL	I2C_SCL
					7	uart_sig_2_sel=0	UART0_RTS	UART0_RTS
						uart_sig_2_sel=1	UART0_CTS	UART0_CTS
						uart_sig_2_sel=2	UART0_TXD	UART0_TXD
						uart_sig_2_sel=3	UART0_RXD	UART0_RXD
					8	-	PWM0_CH0	PWM0_CH0
					10	-	AUADC_CH4	AUADC_CH4
					11	-	SWGPIO10	SWGPIO10
					14	-	TCK	TCK
					21	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					22	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
13	15	AVDD33	DI/DO	PAD_GPIO_11	2	-	-	-
					4	-	SPI_SCLK	SPI_SCLK
					5	-	-	-
					6	-	I2C_SDA	I2C_SDA
					7	uart_sig_3_sel=0	UART0_RTS	UART0_RTS
						uart_sig_3_sel=1	UART0_CTS	UART0_CTS
						uart_sig_3_sel=2	UART0_TXD	UART0_TXD
						uart_sig_3_sel=3	UART0_RXD	UART0_RXD
					8	-	PWM1_CH0	PWM1_CH0
					10	-	ADC_CH10/AUADC_CH5	ADC_CH10/AUADC_CH5
					11	-	SWGPIO11	SWGPIO11
					14	-	TDO	TDO
					21	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					22	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O

Table 3.1: Pin definition(continued)

QFN32	QFN40	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
-	16	AVDD33	DI/DO	PAD_GPIO_12	2	-	-	-
					4	-	SPI_MOSI	SPI_MOSI
					5	-	-	-
					6	-	I2C_SCL	I2C_SCL
					7	uart_sig_0_sel=0	UART0_RTS	UART0_RTS
						uart_sig_0_sel=1	UART0_CTS	UART0_CTS
						uart_sig_0_sel=2	UART0_TXD	UART0_TXD
						uart_sig_0_sel=3	UART0_RXD	UART0_RXD
					8	-	PWM1_CH1	PWM1_CH1
					10	-	ADC_CH11	ADC_CH11
					11	-	SWGPIO12	SWGPIO12
					14	-	TMS	TMS
					21	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					22	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
-	17	AVDD33	DI/DO	PAD_GPIO_13	2	-	-	-
					4	-	SPI_MISO	SPI_MISO
					5	-	-	-
					6	-	I2C_SDA	I2C_SDA
					7	uart_sig_1_sel=0	UART0_RTS	UART0_RTS
						uart_sig_1_sel=1	UART0_CTS	UART0_CTS
						uart_sig_1_sel=2	UART0_TXD	UART0_TXD
						uart_sig_1_sel=3	UART0_RXD	UART0_RXD
					8	-	PWM1_CH2	PWM1_CH2
					10	-	-	-
					11	-	SWGPIO13	SWGPIO13
					14	-	TDI	TDI
					21	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					22	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
20	24	VDDIO_1	DI/DO	PAD_GPIO_14	2	-	-	-
					4	-	SPI_SS	SPI_SS
					5	-	-	-
					6	-	I2C_SCL	I2C_SCL
					7	uart_sig_2_sel=0	UART0_RTS	UART0_RTS
						uart_sig_2_sel=1	UART0_CTS	UART0_CTS
						uart_sig_2_sel=2	UART0_TXD	UART0_TXD
						uart_sig_2_sel=3	UART0_RXD	UART0_RXD
					8	-	PWM1_CH3	PWM1_CH3
					10	-	ADC_CH0/AUADC_CH6	ADC_CH0/AUADC_CH6
					11	-	SWGPIO14	SWGPIO14
					14	-	TCK	TCK
					21	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					22	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
21	25	VDDIO_1	DI/DO	PAD_GPIO_15	2	-	-	-
					4	-	SPI_SCLK	SPI_SCLK
					5	-	-	-
					6	-	I2C_SDA	I2C_SDA
					7	uart_sig_3_sel=0	UART0_RTS	UART0_RTS
						uart_sig_3_sel=1	UART0_CTS	UART0_CTS
						uart_sig_3_sel=2	UART0_TXD	UART0_TXD
						uart_sig_3_sel=3	UART0_RXD	UART0_RXD
					8	-	PWM0_CH0	PWM0_CH0
					10	-	ADC_CH1/AUADC_CH7	ADC_CH1/AUADC_CH7
					11	-	SWGPIO15	SWGPIO15
					14	-	TDO	TDO
					21	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					22	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O

Table 3.1: Pin definition(continued)

QFN32	QFN40	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
22	26	VDDIO_1	DI/DO	PAD_GPIO_16	2	-	-	-
					4	-	SPI_MOSI	SPI_MOSI
					5	-	-	-
					6	-	I2C_SCL	I2C_SCL
					7	uart_sig_0_sel=0	UART0_RTS	UART0_RTS
						uart_sig_0_sel=1	UART0_CTS	UART0_CTS
						uart_sig_0_sel=2	UART0_TXD	UART0_TXD
						uart_sig_0_sel=3	UART0_RXD	UART0_RXD
					8	-	PWM1_CH0	PWM1_CH0
					10	-	-	-
					11	-	SWGPIO16	SWGPIO16
					14	-	TMS	TMS
					21	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					22	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
23	27	VDDIO_1	DI/DO	PAD_GPIO_17	2	-	-	-
					4	-	SPI_MISO	SPI_MISO
					5	-	-	-
					6	-	I2C_SDA	I2C_SDA
					7	uart_sig_1_sel=0	UART0_RTS	UART0_RTS
						uart_sig_1_sel=1	UART0_CTS	UART0_CTS
						uart_sig_1_sel=2	UART0_TXD	UART0_TXD
						uart_sig_1_sel=3	UART0_RXD	UART0_RXD
					8	-	PWM1_CH1	PWM1_CH1
					10	-	ADC_CH2	ADC_CH2
					11	-	SWGPIO17	SWGPIO17
					14	-	TDI	TDI
					21	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					22	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
24	28	VDDIO_1	DI/DO	PAD_GPIO_18	2	-	-	-
					4	-	SPI_SS	SPI_SS
					5	-	-	-
					6	-	I2C_SCL	I2C_SCL
					7	uart_sig_2_sel=0	UART0_RTS	UART0_RTS
						uart_sig_2_sel=1	UART0_CTS	UART0_CTS
						uart_sig_2_sel=2	UART0_TXD	UART0_TXD
						uart_sig_2_sel=3	UART0_RXD	UART0_RXD
					8	-	PWM1_CH2	PWM1_CH2
					10	-	ADC_CH3/IR_TX1	ADC_CH3/IR_TX1
					11	-	SWGPIO18	SWGPIO18
					14	-	TCK	TCK
					21	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					22	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
-	29	VDDIO_1	DI/DO	PAD_GPIO_19	2	-	-	-
					4	-	SPI_SCLK	SPI_SCLK
					5	-	-	-
					6	-	I2C_SDA	I2C_SDA
					7	uart_sig_3_sel=0	UART0_RTS	UART0_RTS
						uart_sig_3_sel=1	UART0_CTS	UART0_CTS
						uart_sig_3_sel=2	UART0_TXD	UART0_TXD
						uart_sig_3_sel=3	UART0_RXD	UART0_RXD
					8	-	PWM1_CH3	PWM1_CH3
					10	-	ADC_CH4	ADC_CH4
					11	-	SWGPIO19	SWGPIO19
					14	-	TDO	TDO
					21	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					22	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O

Table 3.1: Pin definition(continued)

QFN32	QFN40	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
-	30	VDDIO_1	DI/DO	PAD_GPIO_20	2	-	-	-
					4	-	SPI_MOSI	SPI_MOSI
					5	-	-	-
					6	-	I2C_SCL	I2C_SCL
					7	uart_sig_0_sel=0	UART0_RTS	UART0_RTS
						uart_sig_0_sel=1	UART0_CTS	UART0_CTS
						uart_sig_0_sel=2	UART0_TXD	UART0_TXD
						uart_sig_0_sel=3	UART0_RXD	UART0_RXD
					8	-	PWM0_CH0	PWM0_CH0
					10	-	ADC_CH5	ADC_CH5
					11	-	SWGPIO20	SWGPIO20
					14	-	TMS	TMS
					21	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					22	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
-	31	VDDIO_1	DI/DO	PAD_GPIO_21	2	-	-	-
					4	-	SPI_MISO	SPI_MISO
					5	-	-	-
					6	-	I2C_SDA	I2C_SDA
					7	uart_sig_1_sel=0	UART0_RTS	UART0_RTS
						uart_sig_1_sel=1	UART0_CTS	UART0_CTS
						uart_sig_1_sel=2	UART0_TXD	UART0_TXD
						uart_sig_1_sel=3	UART0_RXD	UART0_RXD
					8	-	PWM1_CH0	PWM1_CH0
					10	-	ADC_CH6	ADC_CH6
					11	-	SWGPIO21	SWGPIO21
					14	-	TDI	TDI
					21	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					22	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
25	32	VDDIO_1	DI/DO	PAD_GPIO_22	2	-	-	-
					4	-	SPI_SS	SPI_SS
					5	-	-	-
					6	-	I2C_SCL	I2C_SCL
					7	uart_sig_2_sel=0	UART0_RTS	UART0_RTS
						uart_sig_2_sel=1	UART0_CTS	UART0_CTS
						uart_sig_2_sel=2	UART0_TXD	UART0_TXD
						uart_sig_2_sel=3	UART0_RXD	UART0_RXD
					8	-	PWM1_CH1	PWM1_CH1
					10	-	IR_TX0	IR_TX0
					11	-	SWGPIO22	SWGPIO22
					14	-	TCK	TCK
					21	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					22	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
26	34	VDDIO_1	DI/DO	PAD_GPIO_23 [2]	2	-	SF2_IO0	SF2_IO0
					4	-	SPI_SCLK	SPI_SCLK
					5	-	-	-
					6	-	I2C_SDA	I2C_SDA
					7	uart_sig_3_sel=0	UART0_RTS	UART0_RTS
						uart_sig_3_sel=1	UART0_CTS	UART0_CTS
						uart_sig_3_sel=2	UART0_TXD	UART0_TXD
						uart_sig_3_sel=3	UART0_RXD	UART0_RXD
					8	-	PWM1_CH2	PWM1_CH2
					10	-	-	-
					11	-	SWGPIO23	SWGPIO23
					14	-	TDO	TDO
					21	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					22	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O

Table 3.1: Pin definition(continued)

QFN32	QFN40	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
27	35	VDDIO_1	DI/DO	PAD_GPIO_24 [2]	2	-	SF2_IO2	SF2_IO2
					3	-	SPI_MOSI	SPI_MOSI
					4	-	-	-
					5	-	-	-
					6	-	I2C_SCL	I2C_SCL
					7	uart_sig_0_sel=0	UART0_RTS	UART0_RTS
						uart_sig_0_sel=1	UART0_CTS	UART0_CTS
						uart_sig_0_sel=2	UART0_TXD	UART0_TXD
						uart_sig_0_sel=3	UART0_RXD	UART0_RXD
					8	-	PWM1_CH3	PWM1_CH3
					10	-	-	-
					11	-	SWGPIO24	SWGPIO24
					14	-	TMS	TMS
					21	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					22	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
28	36	VDDIO_1	DI/DO	PAD_GPIO_25 [2]	2	-	SF2_IO1	SF2_IO1
					4	-	SPI_MISO	SPI_MISO
					5	-	-	-
					6	-	I2C_SDA	I2C_SDA
					7	uart_sig_1_sel=0	UART0_RTS	UART0_RTS
						uart_sig_1_sel=1	UART0_CTS	UART0_CTS
						uart_sig_1_sel=2	UART0_TXD	UART0_TXD
						uart_sig_1_sel=3	UART0_RXD	UART0_RXD
					8	-	PWM0_CH0	PWM0_CH0
					10	-	-	-
					11	-	SWGPIO25	SWGPIO25
					14	-	TDI	TDI
					21	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					22	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
29	37	VDDIO_1	DI/DO	PAD_GPIO_26 [2]	2	-	SF2_CS	SF2_CS
					4	-	SPI_SS	SPI_SS
					5	-	-	-
					6	-	I2C_SCL	I2C_SCL
					7	uart_sig_2_sel=0	UART0_RTS	UART0_RTS
						uart_sig_2_sel=1	UART0_CTS	UART0_CTS
						uart_sig_2_sel=2	UART0_TXD	UART0_TXD
						uart_sig_2_sel=3	UART0_RXD	UART0_RXD
					8	-	PWM1_CH0	PWM1_CH0
					10	-	-	-
					11	-	SWGPIO26	SWGPIO26
					14	-	TCK	TCK
					21	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					22	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
30	38	VDDIO_1	DI/DO	PAD_GPIO_27 [2]	2	-	SF2_CLK	SF2_CLK
					4	-	SPI_SCLK	SPI_SCLK
					5	-	-	-
					6	-	I2C_SDA	I2C_SDA
					7	uart_sig_3_sel=0	UART0_RTS	UART0_RTS
						uart_sig_3_sel=1	UART0_CTS	UART0_CTS
						uart_sig_3_sel=2	UART0_TXD	UART0_TXD
						uart_sig_3_sel=3	UART0_RXD	UART0_RXD
					8	-	PWM1_CH1	PWM1_CH1
					10	-	-	-
					11	-	SWGPIO27	SWGPIO27
					14	-	TDO	TDO
					21	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					22	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O

Table 3.1: Pin definition(continued)

QFN32	QFN40	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
31	39	VDDIO_1	DI/DO	PAD_GPIO_28 [2]	2	-	SF2_IO_3	SF2_IO_3
					4	-	SPI_MOSI	SPI_MOSI
					5	-	-	-
					6	-	I2C_SCL	I2C_SCL
					7	uart_sig_0_sel=0	UART0_RTS	UART0_RTS
						uart_sig_0_sel=1	UART0_CTS	UART0_CTS
						uart_sig_0_sel=2	UART0_TXD	UART0_TXD
						uart_sig_0_sel=3	UART0_RXD	UART0_RXD
					8	-	PWM1_CH2	PWM1_CH2
					10	-	-	-
					11	-	SWGPIO28	SWGPIO28
					14	-	TMS	TMS
					21	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					22	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
-	33	VDDIO_1	DI/DO	PAD_GPIO_29	2	-	-	-
					4	-	SPI_MISO	SPI_MISO
					5	-	-	-
					6	-	I2C_SDA	I2C_SDA
					7	uart_sig_1_sel=0	UART0_RTS	UART0_RTS
						uart_sig_1_sel=1	UART0_CTS	UART0_CTS
						uart_sig_1_sel=2	UART0_TXD	UART0_TXD
						uart_sig_1_sel=3	UART0_RXD	UART0_RXD
					8	-	PWM1_CH3	PWM1_CH3
					10	-	-	-
					11	-	SWGPIO29	SWGPIO27
					14	-	TDI	TDI
					21	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					22	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
14	18	AVDD33	DI/DO	PAD_GPIO_30	2	-	-	-
					4	-	SPI_SS	SPI_SS
					5	-	-	-
					6	-	I2C_SCL	I2C_SCL
					7	uart_sig_2_sel=0	UART0_RTS	UART0_RTS
						uart_sig_2_sel=1	UART0_CTS	UART0_CTS
						uart_sig_2_sel=2	UART0_TXD	UART0_TXD
						uart_sig_2_sel=3	UART0_RXD	UART0_RXD
					8	-	PWM0_CH0	PWM0_CH0
					10	-	-	-
					11	-	SWGPIO30	SWGPIO30
					14	-	TCK	TCK
					21	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					22	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
			Analog	XTAL32K_IN	-	-	-	Crystal oscillator 32.768kHz input
15	19	AVDD33	DI/DO	PAD_GPIO_31	2	-	-	-
					4	-	SPI_SCLK	SPI_SCLK
					5	-	-	-
					6	-	I2C_SDA	I2C_SDA
					7	uart_sig_3_sel=0	UART0_RTS	UART0_RTS
						uart_sig_3_sel=1	UART0_CTS	UART0_CTS
						uart_sig_3_sel=2	UART0_TXD	UART0_TXD
						uart_sig_3_sel=3	UART0_RXD	UART0_RXD
					8	-	PWM1_CH0	PWM1_CH0
					10	-	-	-
					11	-	SWGPIO31	SWGPIO31
					14	-	TDO	TDO
					21	-	Key_Scan_In_ROW_I	Key_Scan_In_ROW_I
					22	-	Key_Scan_Drive_COL_O	Key_Scan_Drive_COL_O
			Analog	XTAL32K_OUT	-	-	-	Crystal oscillator 32.768kHz output

Table 3.1: Pin definition(continued)

QFN32	QFN40	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
10	12	AVDD33	Analog	PU_CHIP	-	-	-	Chip power-up
16	20	AVDD_RF	Analog	ANT	-	-	-	RF input and output (single pin)
18	22	AVDD_RF	Analog	XTAL_HF_OUT	-	-	-	External crystal output, 32MHz
19	23	AVDD_RF	Analog	XTAL_HF_IN	-	-	-	External crystal input, 32MHz
32	1	-	Power	VDDIO_1	-	-	-	Externally powered 3.3V or 1.8V
6	8	-	Power	VDDCORE	-	-	-	Internal LDO output (for internal use only)
7	9	-	Power	DCDC_OUT	-	-	-	
8	10	-	Power	SW_DCDC	-	-	-	
9	11	-	Power	AVDD33	-	-	-	Externally powered 3.3V
17	21	-	Power	AVDD_RF	-	-	-	
-	40	-	Power	VDDIO_PSRAM	-	-	-	

[1] This function defaults to SPI_MOSI, which can be converted to SPI_MISO through a register.
[2] BL704L-22-Q2I does not support the use of this pin.

3.1 GPIO initial state

The following table lists the behavior and initial state of each GPIO of BL702L and BL704L when it is powered on (also including releasing reset or waking up from sleep), including default function, direction, pull-up and pull-down, logic level, etc.

Table 3.2: BL702L GPIO initial state

Pin Name	Default Function	Input/Output/Hi-Z	Pull up/down	Logic Level
PAD_GPIO_0	JTAG_TMS			Floating
PAD_GPIO_1	JTAG_TDI			Floating
PAD_GPIO_2	JTAG_TCK			Floating
PAD_GPIO_7	JTAG_TDO			Floating
PAD_GPIO_8	GPIO	Hi-Z		Floating
PAD_GPIO_9	GPIO	Hi-Z		Floating
PAD_GPIO_10	GPIO	Hi-Z		Floating
PAD_GPIO_11	GPIO	Hi-Z		Floating
PAD_GPIO_14	Programming UART TXD			High/Low(Boot)
PAD_GPIO_15	Programming UART RXD			High/Low(Boot)
PAD_GPIO_16	Bootstrap	Input		Floating
PAD_GPIO_17	GPIO			High/Low
PAD_GPIO_18	GPIO	Hi-Z		Floating
PAD_GPIO_22	GPIO	Hi-Z		Floating
PAD_GPIO_23	GPIO	Hi-Z		Floating
PAD_GPIO_24	GPIO	Hi-Z		Floating
PAD_GPIO_25	GPIO	Hi-Z		Floating
PAD_GPIO_26	GPIO	Hi-Z		Floating

Table 3.2: BL702L GPIO initial state(continued)

Pin Name	Default Function	Input/Output/Hi-Z	Pull up/down	Logic Level
PAD_GPIO_27	GPIO	Hi-Z		Floating
PAD_GPIO_28	GPIO	Hi-Z		Floating
PAD_GPIO_30	GPIO			High/Low
PAD_GPIO_31	GPIO	Hi-Z		Floating

Table 3.3: BL704L GPIO initial state

Pin Name	Default Function	Input/Output/Hi-Z	Pull up/down	Logic Level
PAD_GPIO_0	JTAG_TMS			Floating
PAD_GPIO_1	JTAG_TDI			Floating
PAD_GPIO_2	JTAG_TCK			Floating
PAD_GPIO_3	GPIO	Hi-Z		Floating
PAD_GPIO_7	JTAG_TDO			Floating
PAD_GPIO_8	GPIO	Hi-Z		Floating
PAD_GPIO_9	GPIO	Hi-Z		Floating
PAD_GPIO_10	GPIO	Hi-Z		Floating
PAD_GPIO_11	GPIO	Hi-Z		Floating
PAD_GPIO_12	GPIO	Hi-Z		Floating
PAD_GPIO_13	GPIO	Hi-Z		Floating
PAD_GPIO_14	Programming UART TXD			High/Low(Boot)
PAD_GPIO_15	Programming UART RXD			High/Low(Boot)
PAD_GPIO_16	Bootstrap	Input		Floating
PAD_GPIO_17	GPIO			High/Low
PAD_GPIO_18	GPIO	Hi-Z		Floating
PAD_GPIO_19	GPIO	Hi-Z		Floating
PAD_GPIO_20	GPIO	Hi-Z		Floating
PAD_GPIO_21	GPIO	Hi-Z		Floating
PAD_GPIO_22	GPIO	Hi-Z		Floating
PAD_GPIO_23	GPIO	Hi-Z		Floating
PAD_GPIO_24	GPIO	Hi-Z		Floating
PAD_GPIO_25	GPIO	Hi-Z		Floating
PAD_GPIO_26	GPIO	Hi-Z		Floating
PAD_GPIO_27	GPIO	Hi-Z		Floating
PAD_GPIO_28	GPIO	Hi-Z		Floating

Table 3.3: BL704L GPIO initial state(continued)

Pin Name	Default Function	Input/Output/Hi-Z	Pull up/down	Logic Level
PAD_GPIO_29	GPIO	Hi-Z		Floating
PAD_GPIO_30	GPIO			High/Low
PAD_GPIO_31	GPIO	Hi-Z		Floating

Note: In PWM lighting control applications, the IO that generates the PWM needs to be kept in a certain state (usually low) during the power-on process to avoid flickering.

1. GPIO17 and GPIO30 will output high and low levels during power-up, so they are not recommended to be used as PWM light control;
2. Other GPIOs are used for PWM light control. It is recommended to reserve the pull-down resistor to avoid floating state.

4 RF Characteristsic

RF Characteristics of Receiving and Transmitting modes.

Table 4.1: BLE RX RF characteristics

Mode		Note	Performance @3.3V,25°C			
			Min.	Typ	Max.	Unit
Receiver Sensitivity	1Mbps	packet length 37bytes, dirty transmitter off		-97.5		dBm
	2Mbps			-95		
Maximum Input Level	1Mbps			> 5		
	2Mbps			> 5		

Table 4.2: BLE TX RF characteristics

Mode		Note	Performance @3.3V,25°C			
			Min.	Typ	Max.	Unit
Modulation Characteristics	1Mbps, Δf1avg			251		KHz
	1Mbps, Δf2max 99.9%			>200		
	1Mbps, Δf2avg/Δf1avg			0.87		
	2Mbps, Δf1avg			499		KHz
	2Mbps, Δf2max 99.9%			>400		
	2Mbps, Δf2avg/Δf1avg			0.87		
Carrier Frequency Offset and Drift	1Mbps, $\lvert f_n \rvert$			<20		KHz
	1Mbps, $\lvert f_0 - f_n \rvert$			< 5		
	1Mbps, $\lvert f_1 - f_0 \rvert$			< 5		
	1Mbps, $\lvert f_n - f_{(n-5)} \rvert$			< 2		
	2Mbps, $\lvert f_n \rvert$			< 20		
	2Mbps, $\lvert f_0 - f_n \rvert$			< 5		

Table 4.2: BLE TX RF characteristics(continued)

Mode		Note	Performance @3.3V,25°C			
			Min.	Typ	Max.	Unit
	2Mbps, $\|f_1 - f_0\|$			< 5		
	2Mbps, $\|f_n - f_{(n-5)}\|$			< 2		
In-Band Emission	1Mbps, F = F_0± 2MHz			-31		dBm
	1Mbps, F = F_0± 3MHz			-42		
	2Mbps, F = F_0± 4MHz			-48		
	2Mbps, F = F_0± 5MHz			-50		
	2Mbps, F = F_0± 6MHz			< -50		
Output Power	1Mbps			9	10	dBm
	2Mbps			9	10	

Table 4.3: ZigBee RX RF characteristics

Mode		Note	Performance @3.3V,25°C			
			Min.	Typ	Max.	Unit
Rx Sensitivity	250Kbps			-103		dBm

Table 4.4: ZigBee TX RF characteristics

Mode		Note	Performance @3.3V,25°C			
			Min.	Typ	Max.	Unit
Transmit Power	250Kbps			9	10	dBm
EVM	250Kbps			14		%

5 Power Consumption

Power Consumption of each power mode.

Table 5.1: Power Modes & Whole-chip Current

Mode	Conditions	Performance @25℃			
		Min.	Typ	Max.	Unit
RX	BLE 1Mbps, Rx power = -70dBm		4.8		mA
TX	BLE 1Mbps, Tx power = 9dBm		20		
	BLE 1Mbps, Tx power = 0dBm		5.2		
Power Down Sleep	PDS31, with low power mode enabled		2.8		uA
Hibernate	HNB0, with low power mode enabled		1		
Shut-down	PU_CHIP = low		0.1		

6 Electrical Specifications

6.1 Absolute Maximum Rating

Table 6.1: Absolute Maximum Rating

Pin Name	Min.	Max.	Unit
AVDD33, VDDIO_1	-0.3	3.63	V
ESD Protection (HBM)	2000		V
Storage Temperature	-40	125	°C

6.2 Operating Condition

6.2.1 Power characteristics

Table 6.2: Recommended Power Operating Range

Pin Name	Min.	Typ	Max.	Unit
AVDD33, VDDIO_1	1.8 [1]	3.3	3.63	V

[1] The minimum operating voltage of the main chip is 1.8V. For Flash/pSRAM co-packaged chips, the minimum operating voltage is related to the minimum operating voltage of Flash/pSRAM, which is mostly 2.7V, and wide voltage version (voltage range code = W) can support 1.8V.

6.2.2 IO DC characteristics

Test conditions:VDDIO = 3.3V, temperature = 25°C

Table 6.3: IO DC characteristics

Sym-bol	Descrip-tion	GPIO num	Conditions	Min.	Typ	Max.	Unit
VOH	Output voltage high	All GPIO	GPIO drive strength 0, source current = 2.9mA		0.9*VDDIO		V
			GPIO drive strength 1, source current = 8.5mA				
			GPIO drive strength 2, source current = 16.8mA				
			GPIO drive strength 3, source current = 22.2mA				
VOL	Output voltage low	All GPIO	GPIO drive strength 0, sink current = 3.1mA		0.1*VDDIO		V
			GPIO drive strength 1, sink current = 9.2mA				
			GPIO drive strength 2, sink current = 18.2mA				
			GPIO drive strength 3, sink current = 24mA				
VIH	Input voltage high	All GPIO		0.7*VDDIO			V
VIL	Input voltage low	All GPIO				0.3*VDDIO	V

6.2.3 Power-on sequence

In order to ensure normal power-on startup, the power, reset and Bootstrap pins need to meet the corresponding timing requirements.

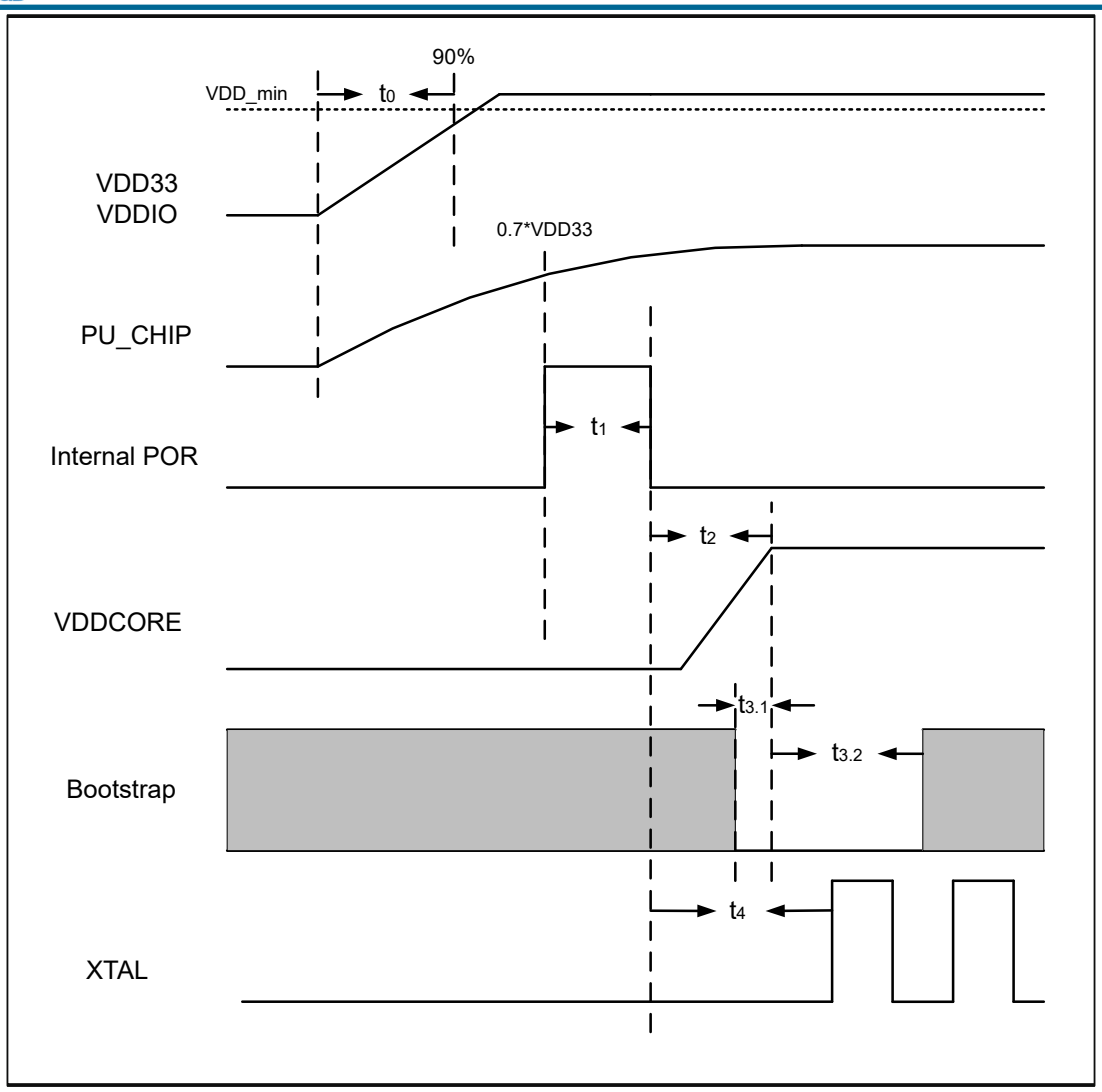


Fig. 6.1: Power-on sequence

Table 6.4: Power-on sequence parameters

Parameters	Description	Min.(ms)	Typ(ms)	Max.(ms)
t_0	The power supply voltage reaches 90% rise time [1]		0.1	
t_1	Internal POR duration		2.5	
t_2	VDDCORE setting time after Internal POR down		1	
$t_{3.1}$	Bootstrap pin [2]preparation time before VDDCORE establishment	0		
$t_{3.2}$	Duration of valid voltage level at the Bootstrap pin.	2		
t_4	XTAL startup time after Internal POR down		1	

[1] VDD_min is the minimum value for proper chip operation.

[2] Bootstrap pin is GPIO16.

6.2.4 Shutdown Sequence

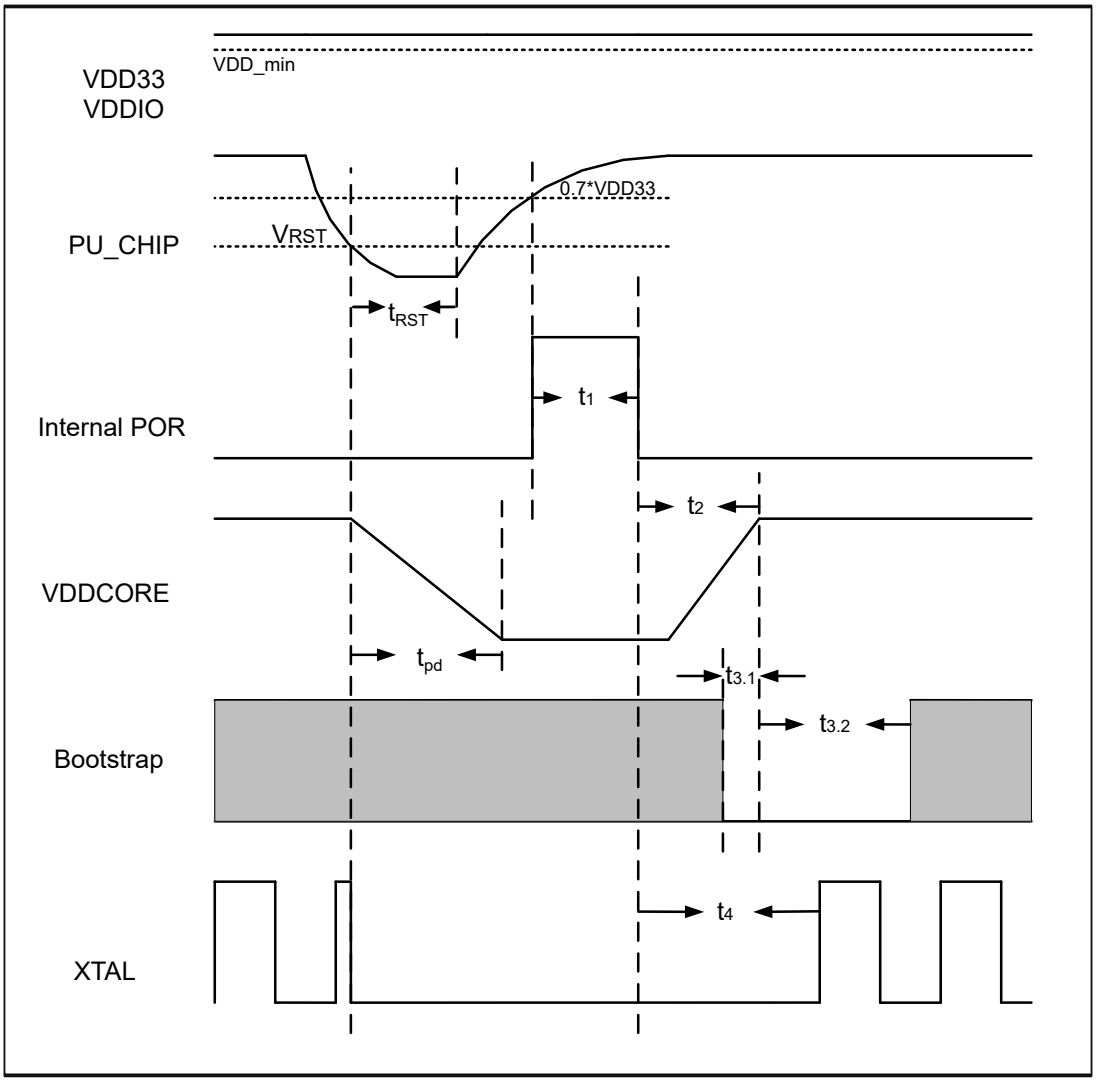


Fig. 6.2: Shutdown sequence

Table 6.5: Shutdown sequence parameters

Parameters	Description	Min.	Typ	Max.	Unit
V_{RST}	Shutdown occurs after PU_CHIP lower than this voltage	0	0.1*VDD33	0.3*VDD33	V
t_{RST}	The required time that PU_CHIP lower than V_{RST}	1	1		ms
t_{pd}	Time for VDDCORE to decrease to 0 after shutdown	1	1		ms

6.2.5 Temperature characteristics

Table 6.6: Recommended Temperature Operating Range

Item		Min.	Max.	Unit
Temperature	Main Die	-40	105	°C
	Multi-Die SiP(Flash, Psram)	-40	85 [1]	°C

[1] The maximum temperature of BL704L-22-Q2H is 105°C.

6.2.6 General operating conditions

Table 6.7: General Operating Conditions

Item	Description	Min.	Typ	Max.	Unit
FCPU	CPU/TCM/Cache clock frequency		32	128	MHz
FBUS	System bus clock frequency		32	64	MHz

6.2.7 GPADC characteristics

Table 6.8: GPADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VDD	Supply voltage		1.8		3.63	V
T	Working tempreture		-40		105	°C
I_{vdd}	Current consumption	PGA1&2 off (2M clock)		150		μA
		PGA1&2 on(2M clock)		350		
Fclk	ADC input top clock frequency	Clock from SOC	1.5		32	MHz
Fsample	Sampling rate	2M(12bit mode) 31.25K-125K(14bit mode) 7.8125K-15.625K(16bit mode)			1	MHz
Vin	Input voltage range	Differential mode			5.8	V(vpp)
		Single-ended mode			2.9	
Rin	Total input channel resistance				2	KΩ
Tpu	Power up time				1	uS

Table 6.8: GPADC characteristics(continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Tconv	Total conversion time	12bit mode			1	1/Fsample
		14bit mode [1]			16	
		14bit mode [2]			64	
		16bit mode [3]			128	
		16bit mode [4]			256	

[1] 14-bit mode with 16 times average
[2] 14-bit mode with 64 times average
[3] 16-bit mode with 128 times average
[4] 16-bit mode with 256 times average

Table 6.9: ADC electrical characteristic

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DNL	Differential linearity error				+/-1	LSB
INL	Integral linearity error				+/-2	LSB
Offset	Input offset				+/-2	LSB
Ge [1]	Gain error				+/-1	%
ENOB	Effective number of bits	12bit mode(201KHz input)	9.7	10.5		bit
		14bit mode(2.5KHz input)	10.8	11.4		
		16bit mode(1KHz input)	11.5	12.3		
SNDR	Signal-to-noise-distortion (PGA gain=1)	12bit mode(201KHz input)	59	65		dB
		14bit mode(2.5KHz input)	66	72.4		
		16bit mode(1KHz input)	71	76.8		
SNDR	Signal-to-noise-distortion (PGA gain=4)	12bit mode(201KHz input)	58	64		dB
		14bit mode(2.5KHz input)	64	69.5		
		16bit mode(1KHz input)	70	74		

[1] after calibration

7 Product use

7.1 Moisture Sensitivity Level(MSL)

The moisture sensitivity level of the chip is: MSL3. After the vacuum package is opened, it needs to be used up within 168 hours (7 days) at ≤30°C/60%RH, otherwise it needs to be baked and put online.

For baking temperature and time, please refer to IPC/JEDECJ-STD-033B01.

Table 7.1: Reference Conditions for Drying Mounted or Unmounted SMD Packages (User Bake: Floor life begins counting at time = 0 after bake)

Package Body	Level	Bake @ 125°C		Bake @ 90°C ≤5% RH		Bake @ 40°C ≤5% RH	
		Exceeding Floor Life by >72 h	Exceeding Floor Life by ≤72 h	Exceeding Floor Life by >72 h	Exceeding Floor Life by ≤72 h	Exceeding Floor Life by >72 h	Exceeding Floor Life by ≤72 h
Thickness ≤1.4 mm	2	5 hours	3 hours	17 hours	11 hours	8 days	5 days
	2a	7 hours	5 hours	23 hours	13 hours	9 days	7 days
	3	9 hours	7 hours	33 hours	23 hours	13 days	9 days
	4	11 hours	7 hours	37 hours	23 hours	15 days	9 days
	5	12 hours	7 hours	41 hours	24 hours	17 days	10 days
	5a	16 hours	10 hours	54 hours	24 hours	22 days	10 days

7.2 Electro-Static discharge（ESD）

- Human Body Model(HBM): 2000V
- Charged-Device Model(CDM): 500V

7.3 Reflow Profile

For details, please refer to IPC/JEDEC J-STD-020E.

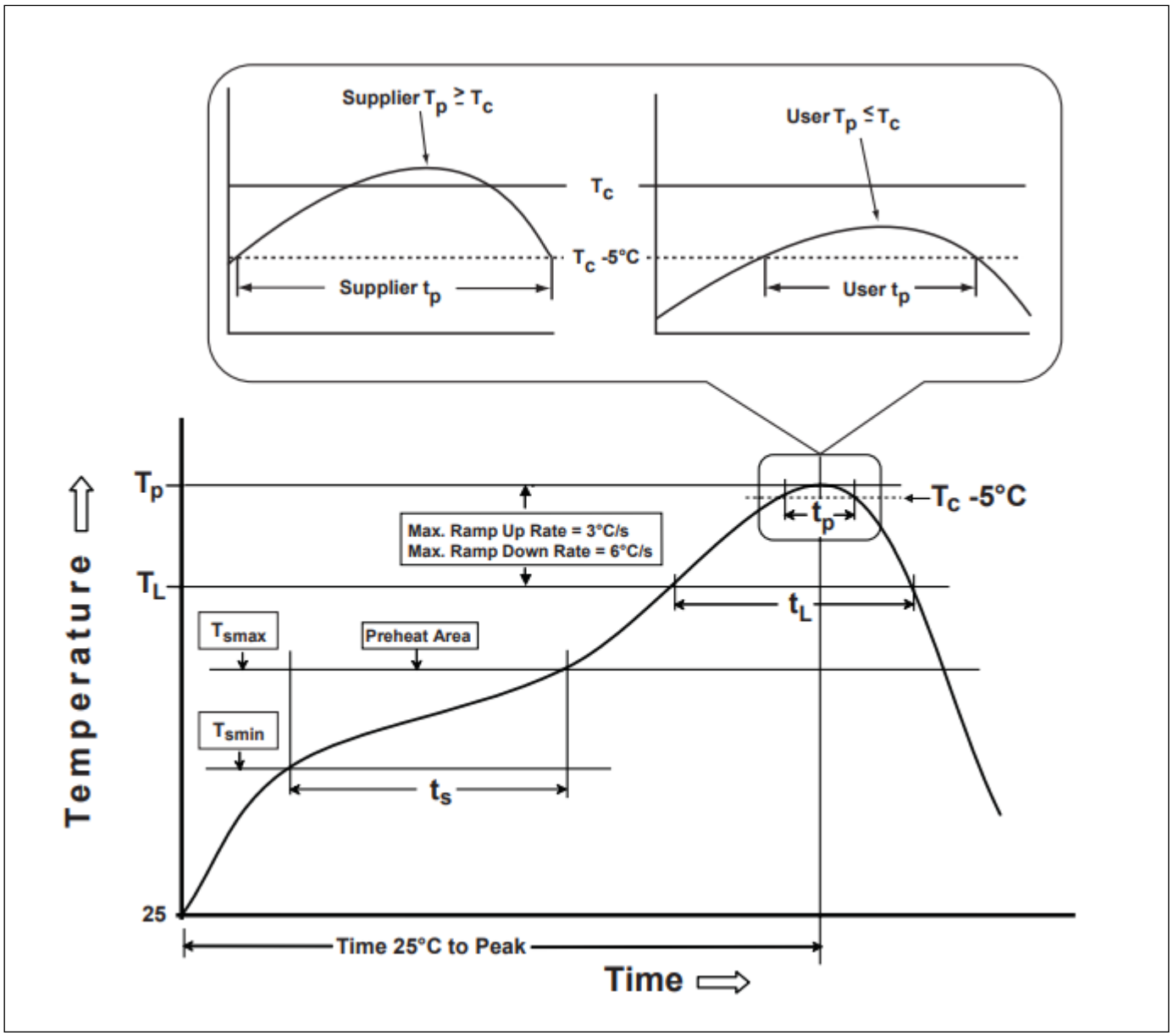
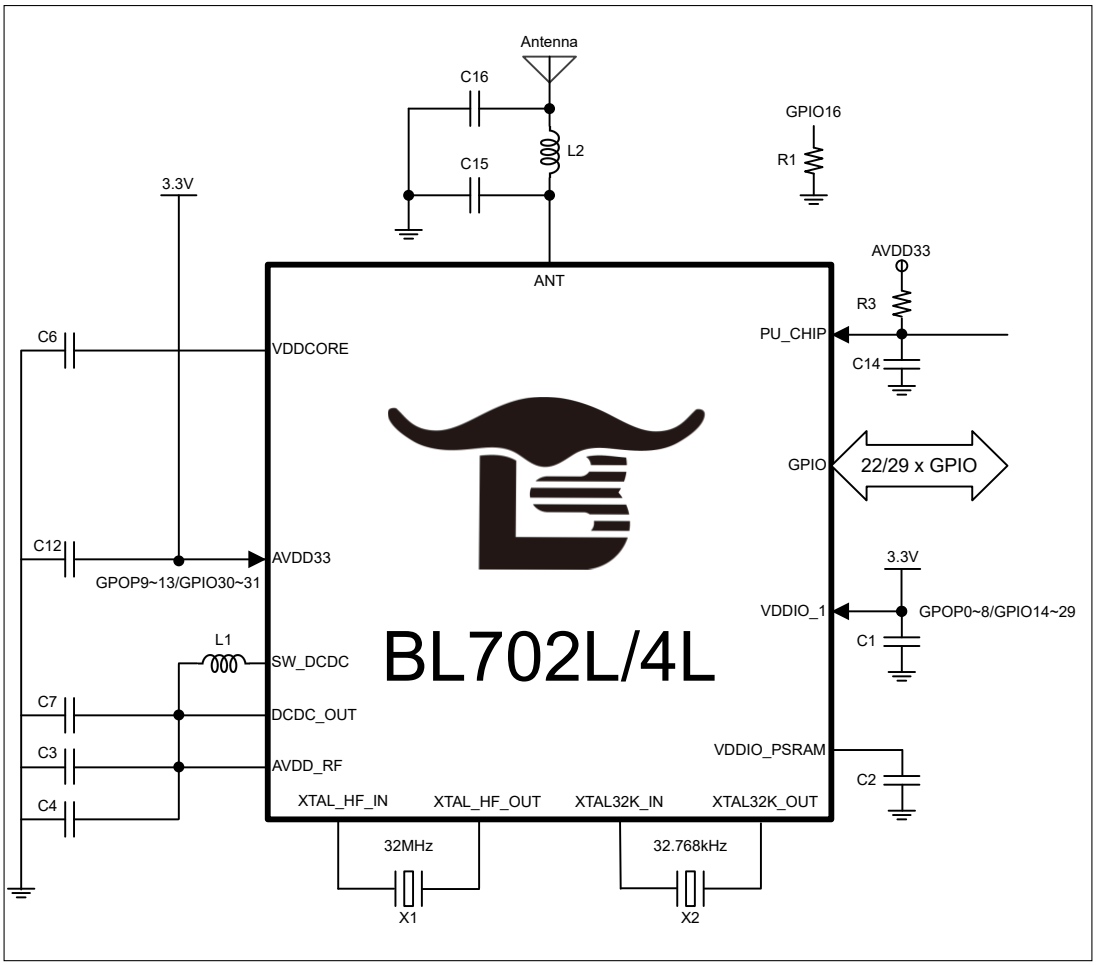


Fig. 7.1: Classification Profile (Not to scale)

Table 7.2: Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat/Soak Temperature Min (T_{smin}) Temperature Max (T_{smax}) Time (t_s) from (T_{smin} to T_{smax})	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Ramp-up rate (T_L to T_p)	3 °C/second max.	3 °C/second max.
Liquidous temperature (T_L) Time (t_L) maintained above T_L	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body temperature (T_p)	240 °C+0/-5 °C	250 °C+0/-5 °C
Time (t_p)* within 5 °C of the specified classification temperature (T_c)	10-30 seconds	20-40 seconds
Ramp-down rate (T_p to T_L)	6 °C/second max	6 °C/second max
Time 25 °C to peak temperature	6 minutes max	8 minutes max
- Tolerance for peak profile temperature (Tp) is defined as a supplier minimum and a user maximum.		

8 Reference Design



9 Package Information(QFN32)

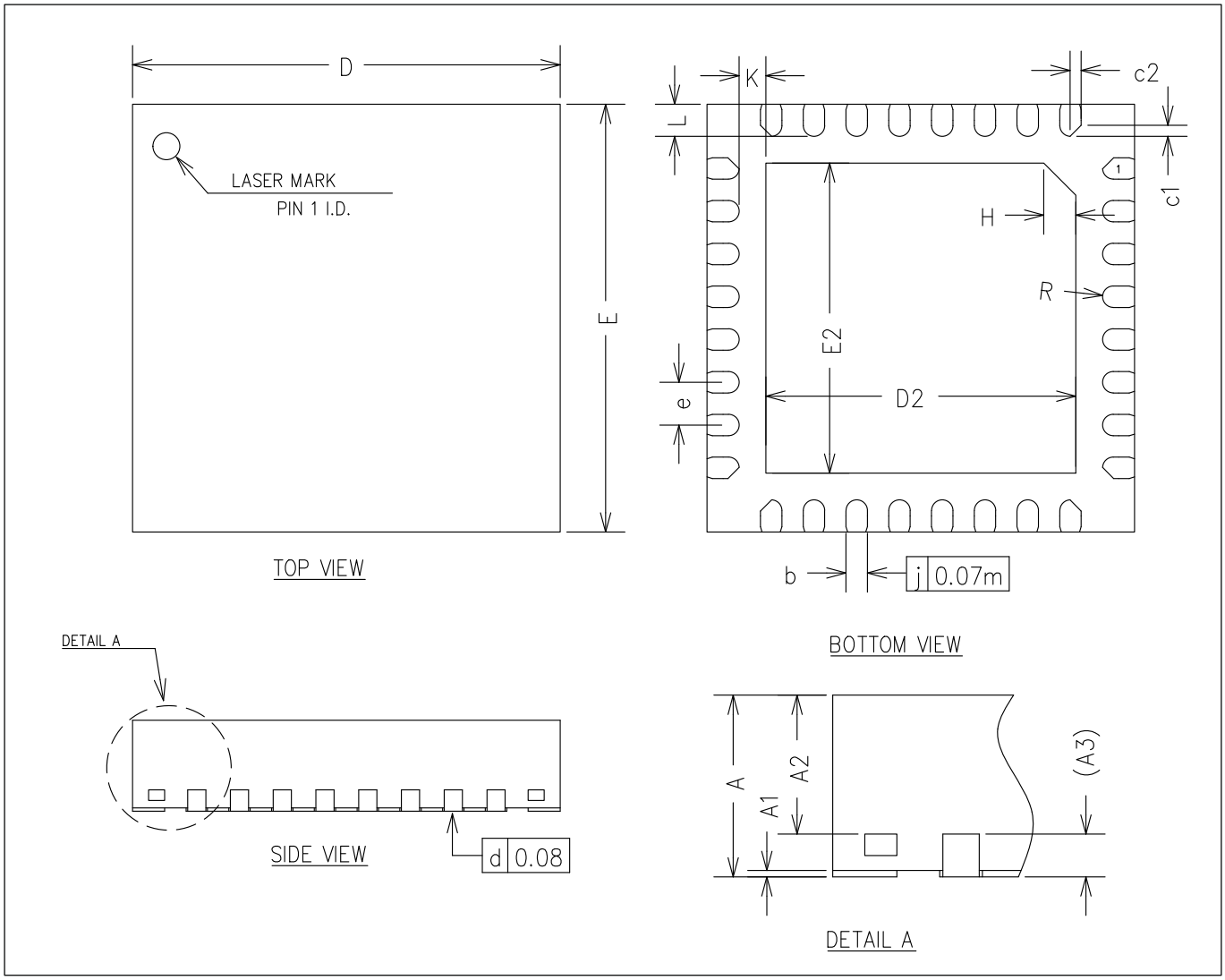


Fig. 9.1: QFN32 Package drawing

Table 9.1: QFN32 Size Description

SYMBOL	UNIT OF MEASURE = MILLIMETER		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A2	0.60	0.65	0.70
A3	0.20REF		
b	0.15	0.20	0.25
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.80	2.90	3.00
E2	2.80	2.90	3.00
e	0.30	0.40	0.50
H	0.30REF		
K	0.25REF		
L	0.25	0.30	0.35
R	0.09	-	-
c1	-	0.10	-
c2	-	0.10	-

10 Package Information(QFN40)

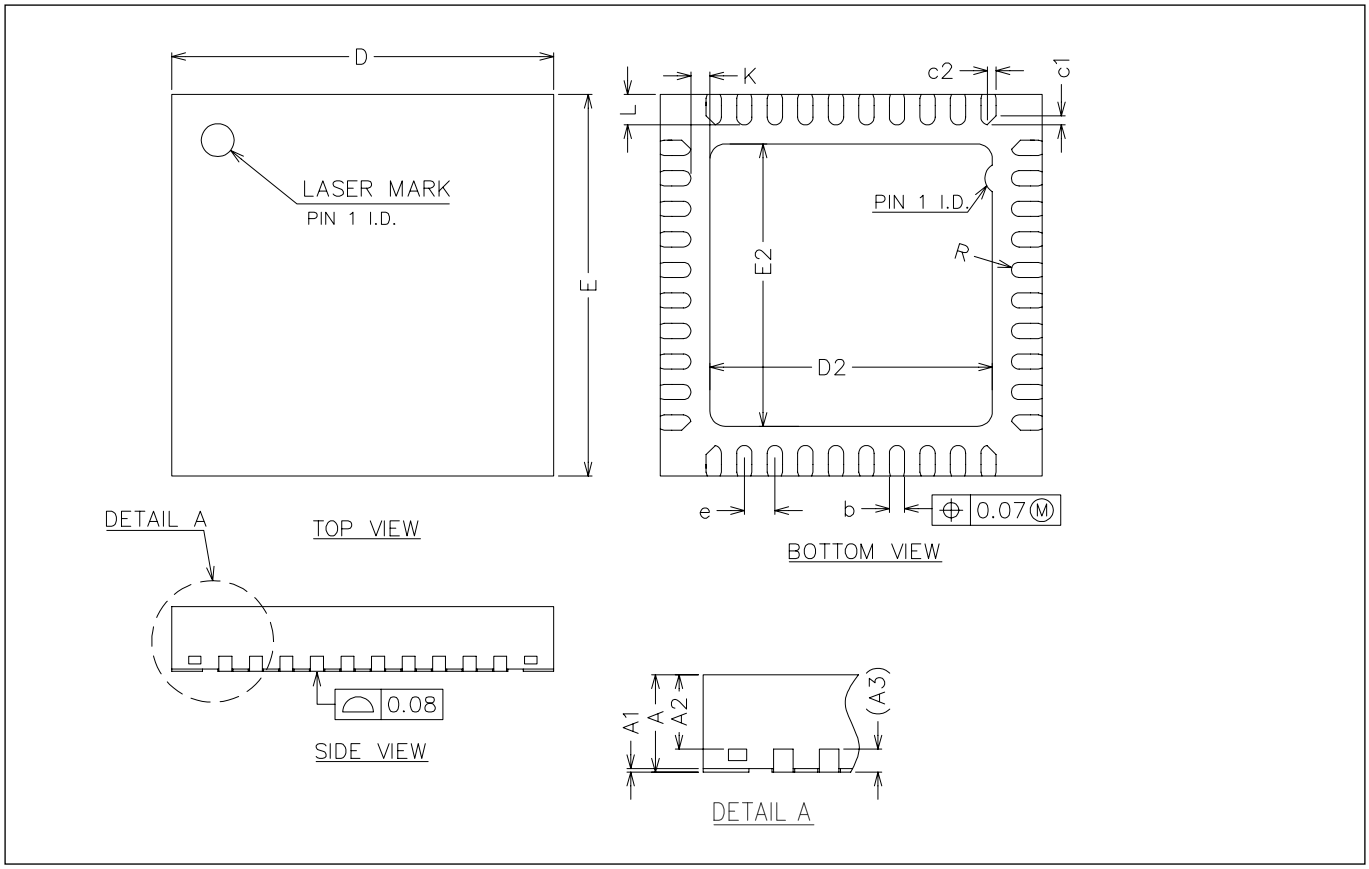


Fig. 10.1: QFN40 Package drawing

Table 10.1: QFN40 Size Description

SYMBOL	UNIT OF MEASURE = MILLIMETER		
	MIN	NOM	MAX
A	0.80	0.85	0.90

Table 10.1: QFN40 Size Description(continued)

SYMBOL	UNIT OF MEASURE = MILLIMETER		
	MIN	NOM	MAX
A1	0.00	0.02	0.05
A2	0.60	0.65	0.70
A3	0.20 REF		
b	0.15	0.20	0.25
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D2	3.60	3.70	3.80
E2	3.60	3.70	3.80
e	0.35	0.40	0.45
K	0.20	-	-
L	0.35	0.40	0.45
R	0.075	-	-
c1	-	0.12	-
c2	-	0.12	-

11 Top Marking Definition

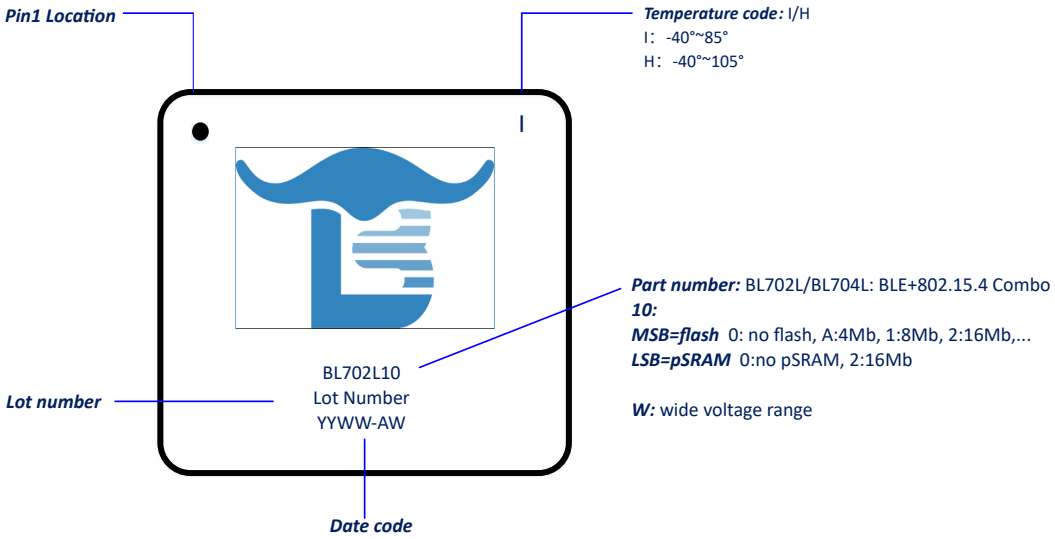


Fig. 11.1: Top Marking Definition

12 Ordering Information

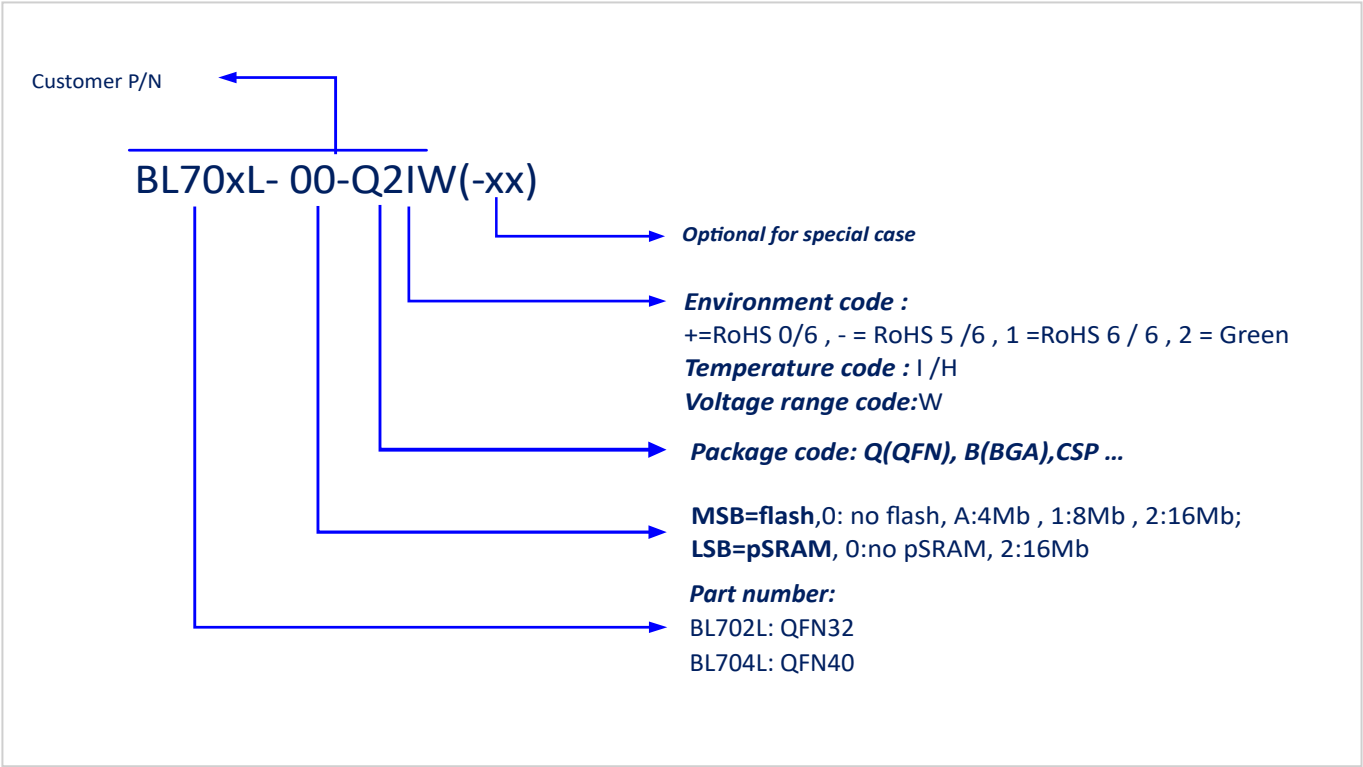


Fig. 12.1: Part Number

Table 12.1: Part Order Options

Customer P/N	Type	Package Size(mm)	MOQ	Description
BL702L-10-Q2I	QFN32	4x4x0.85, Pitch 0.4	6K	BLE+802.15.4 Combo, 8Mb Flash
BL704L-22-Q2H	QFN40	5x5x0.85, Pitch 0.4	6K	BLE+802.15.4 Combo, 16Mb Flash, 16Mb pSRAM
BL704L-10-Q2IW	QFN40	5x5x0.85, Pitch 0.4	6K	BLE+802.15.4 Combo, 8Mb Flash, wide voltage range 1.8V ~ 3.6V

Table 12.1: Part Order Options(continued)

Customer P/N	Type	Package Size(mm)	MOQ	Description
BL704L-20-Q2IW	QFN40	5x5x0.85, Pitch 0.4	6K	BLE+802.15.4 Combo, 16Mb Flash, wide voltage range 1.8V ~ 3.6V
BL702L-A0-Q2I	QFN32	4x4x0.85, Pitch 0.4	6K	BLE+802.15.4 Combo, 4Mb Flash

Table 12.2: Product Packaging Information

Package Size(mm)	Reel size	Quantity per Master Carton	Quantity per Roll	Reel Diameter	Tape Width	Tape Pitch	Moisture Sensitivity Level	Package Type
QFN 4*4	13”	30000	6000	330mm	12mm	8mm	MSL3	Tape reel
QFN 5*5	13”	30000	6000	330mm	12mm	8mm	MSL3	

13 Revision history

Table 13.1: Document revision history

Date	Revision	Changes
2023/1/19	0.5	Initial release
2023/3/22	1.0	Add description of power characteristics
2023/3/28	1.1	Update Flash voltage description in the power characteristics section
2023/5/5	1.2	Add GPIO pin description of BL704L-22-Q2I
2023/5/22	1.3	Modify PWM v1 and PWM v2 pin function descriptions
2023/8/24	1.4	Add AUADC and IR pin functional description
2023/10/12	1.5	1.Add GPIO initial state 2.Update GPIO VOH/VOL characteristics 3.Add BL704L-10-Q2I ordering information
2023/10/26	1.6	1.Add notes for the initial state of GPIO 2.Add BL704L-10-Q2IW description
2024/1/8	1.7	Modify power-on sequence and shutdown sequence
2024/4/12	1.8	Add BL704L-20-Q2IW ordering information
2024/5/22	1.9	1.Update GPADC characteristics 2.Add OCRAM and ITCM description
2024/5/28	2.0	Add Product Packaging Information
2025/2/25	2.1	Add BL702L-A0-Q2I ordering information